Integrated Power Electronic Converters *and* Digital Control

Ali Emadi
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Dedications

To my family

Ali Emadi

To my father, mother, and brother

Alireza Khaligh

To my father, mother, brother, and wife

Zhong Nie

To my wife and daughter

Young-Joo Lee

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Preface

With the demand for higher efficiencies, smaller output ripple, and smaller converter size for modern power electronic systems, conventional switched-mode power supplies could be replaced by integrated power electronic converters. An integrated converter is a synthesized device based on the overall system integration, which is simplified by the system objective and can implement the system functions similar to the discrete converters without integration. Based on the requirements of the design, integrated converters have reduced components, smaller size, lower weight, lower cost, higher efficiency, higher reliability, lower switching stresses, smaller power packing, wide conversion range, power factor correction and output regulation, and better performance.

The first 14 chapters of this book describe various integrated power electronic converters such as boost type, buck type, and buck-boost type integrated topologies, as well as other integrated structures. Steady-state and dynamic analyses of boost integrated flyback rectifier/energy storage DC-DC (BIFRED) converters and buck integrated forward converters are then presented. Introduction to the non-isolated DC-DC converters such as buck, boost, and buck-boost converters are presented in Chapter 1. Chapter 2 is an introduction to the isolated DC-DC converters such as flyback, forward, push-pull, full-bridge, and half-bridge converters. In Chapter 3, the basic concept of power factor correction and its application to buck, boost, buck-boost, Ćuk, single-ended primary inductor (SEPIC), zeta, flyback, and forward converters is explained. Chapter 4 addresses the concept of integrated converters and definition of the integrated switched-mode power supplies. Chapters 5, 6, and 7 describe boost-type, buck-type, and buck-boost–type integrated topologies. Other types of integrated topologies are presented in Chapter 8.

A steady-state analysis of the boost integrated flyback rectifier energy storage converter is demonstrated in Chapter 9. Chapter 10 presents the dynamic analysis of the buck integrated forward converter. Chapter 11 is an introductory chapter to the concept of synchronous rectification and its application to the non-isolated DC-DC buck, boost, and buck-boost converters. Application of synchronous rectification to the isolated DC-DC

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converters such as flyback and forward converters is presented in Chapter 12. Chapter 13 presents the application of synchronous rectification to the integrated high-quality rectifier-regulators. In addition, Chapter 14 demonstrates the application of the integrated switched-mode power converters for uninterruptible power supply and switched reluctance motor drive applications.

The last two chapters of the book describe digital control based on digital signal processors (DSPs). Over the past several years, digital control based on general purpose microprocessors, application-specific integrated circuits, DSPs, or programmable logic devices have become pervasive in power electronic applications. Specially, significant commercial strides have been made in digital power management and control. Power electronics-based companies have started introducing products that integrate digital power management and control integrated circuit solutions, both hybrid (analog and digital) and pure digital. In the meantime, system makers are looking seriously at the benefits of digital control and coming up with their own, often proprietary, products. These trends are occurring at various levels of implementation such as power conversion, converter management, board management, and rack management, which is in fact digital power management of the system. Cost, space, flexibility, energy efficiency, and voltage regulation are the key factors in digital power management and implementation.

This book addresses various applications of the digital control techniques for power electronic converters and provides details of implementing digital control techniques using DSPs. Chapter 15 presents a comprehensive literature study of the digital control techniques in power electronics. Finally, in Chapter 16, after an introduction to the implementation of the digital control techniques using DSPs, the hardware and software implementation of a non-inverting buck-boost converter is explained in detail.

This book is recommended as a reference text for an advanced course in power electronics. This book is also an in-depth source for engineers, researchers, and managers who are working in power electronics and related industries.

We would like to gratefully acknowledge the contributions of Mr. Ritesh Oza. Chapters 3, 11, 12, and 13 draw heavily from his graduate research work at Illinois Institute of Technology. We would also like to acknowledge the efforts and assistance of the staff of CRC Press–Taylor & Francis Group.

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chapter one

Non-isolated DC-DC Converters

The DC-DC converters are widely used in regulated switched-mode DC power supplies and DC motor drive applications. The input to these converters is often an unregulated DC voltage, which is obtained by rectifying the line voltage, and therefore it will fluctuate due to changes in the line voltage magnitude. Switched-mode DC-DC converters are used to convert the unregulated DC input to a controlled DC output at a desired voltage level [1].

The converters are very often used with an electrical isolation transformer in the switched-mode DC power supplies and almost always without an isolation transformer in the case of DC motor drives [2].

Buck (step down), boost (step up) converters and buck-boost are the basic converter topologies. There is a very wide choice of topologies available; each one has its own particular advantages and disadvantages, making it suitable for special power supply application [1]-[6]. Basic operation, advantages, drawbacks, and most common area of use for the most common topologies are discussed in the following sections.

1.1 Buck Converter

This is one of the non-isolated, very basic switching power supply topologies [3], [4]. The output voltage in this topology is always less than the input voltage and thus it is considered a buck converter. The power stage circuit is shown in Figure 1.1.

Depending on the current through the inductor L, the converter can be operated in two basic operating modes. One of them is continuous conduction mode (CCM) and the other is discontinuous conduction mode (DCM). The converter is said to be in CCM when the current through the inductor never reaches zero (for example, i_L is always positive). On the other hand, if the inductor current reaches zero and stays zero for some time, the converter is said to be in DCM. The boundary between continuous and discontinuous conduction mode is known as critical continuous conduction mode (CCCM) or critical discontinuous conduction mode (CDCM).

When switch S is turned on, the input voltage is applied to inductor L and power is delivered to the output. Inductor current also builds up according to Faraday's law. When the switch is turned off, the voltage

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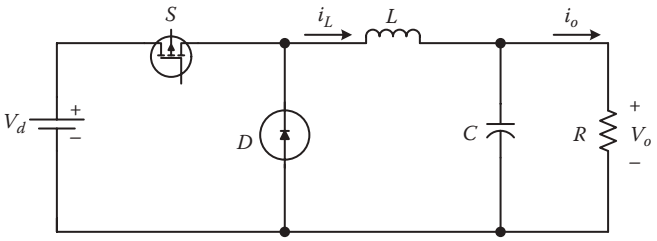


Figure 1.1 Buck converter.

across the inductor reverse and freewheel diode D becomes forward biased. This allows the energy stored in the inductor to be delivered to the output. This continuous current is then smoothed by output capacitor C.

The LC filter has an averaging effect on the applied pulsating input, producing a smooth DC output voltage and current, with very small ripple components superimposed. The average voltage-second across the inductor over a completer switch cycle must equal zero in the steady state.

1.1.1 Buck Converter in Continuous Conduction Mode

The operating mode starts when the switch is turned on. Here it is assumed that the converter is in continuous conduction mode and thus, initially, the inductor current is holding some minimum value. When the switch is on, negative voltage appears across the diode and it turns to off. Therefore, the current goes through the inductor. The inductor current increases linearly or, in other words, the inductor is charged in this sub-interval. The power stage circuit for the converter in this operating mode is shown in Figure 1.2.

This sub-interval comes to an end when the switch is off. This off command may come from the control circuit. Once the switch is off, the inductor current will force the diode to conduct. The inductor current starts decreasing. The power stage circuit in this mode is shown in Figure 1.3.

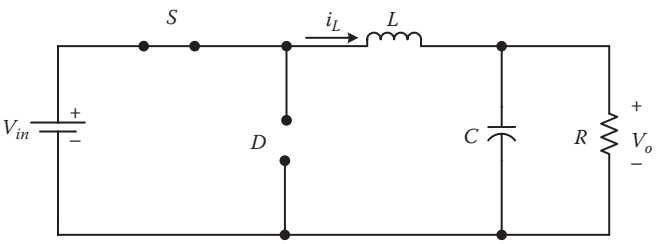


Figure 1.2 Buck converter when switch S is on.

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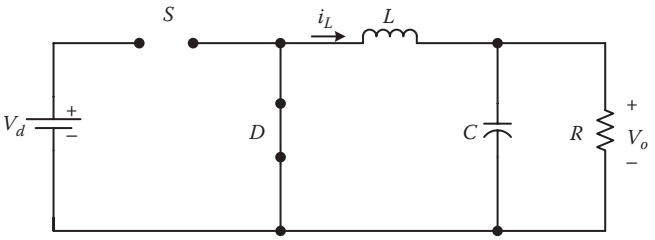


Figure 1.3 Buck converter when switch S is off.

Inductor current continues to decrease in this sub-interval. As mentioned earlier, it is assumed that the converter is operating in CCM. Thus, any time before the inductor current hits zero, the switch must be on. As soon as the switch returns to on, this mode comes to an end and the inductor current again starts increasing. And the cycle repeats itself.

1.1.2 Buck Converter in Discontinuous Conduction Mode

From the definition of the DCM, the converter is said to be in DCM when the inductor current reaches zero and stays zero for some time. Thus, when the converter operates in DCM the above mentioned two sub-intervals remain the same. The difference will be in the second sub-interval. The inductor current here decreases to zero and tries to be negative, but the diode becomes reverse biased and stops conducting. The converter then enters into a third sub-interval where inductor current is zero for some time and the load is supplied entirely from the output capacitor. The mode comes to an end when the switch is on and the inductor current again starts increasing from zero (unlike continuous conduction mode, where initial inductor current has some minimum value). The power stage circuit for the first two modes remains the same and the third mode power stage is shown in Figure 1.4.

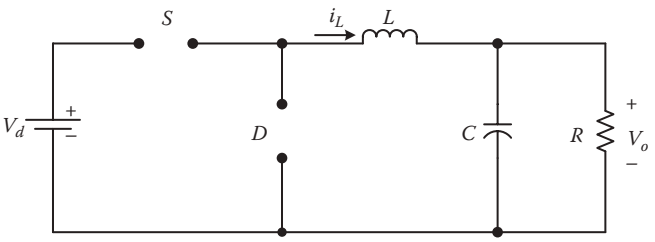


Figure 1.4 Buck converter when both switch S and diode D are off.

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1.1.3 Design Considerations for Buck Converter

To operate the converter in any particular desired mode, its components are to be designed in a specific way. Here, as mentioned before, the inductor current decides the operating mode, and thus the inductor must be designed in such a way that the converter operates in CCM or DCM, whichever is desired (Figures 1.5 and 1.6). The capacitor is to be designed to give a particular amount of ripple in the output voltage [4]. To achieve these inductance and capacitance values steady-state equations for the converter have to be solved in each sub-interval of the switching period.

Here the complete procedure for the buck converter is explained. As it is not possible to cover every detail, for the rest of the topologies the final design values will be given directly.

The first sub-interval, for example, from switch on to switch off can be written as,

$$0 < t < DT \tag{1.1}$$

$$V_d = v_L + V_o \tag{1.2}$$

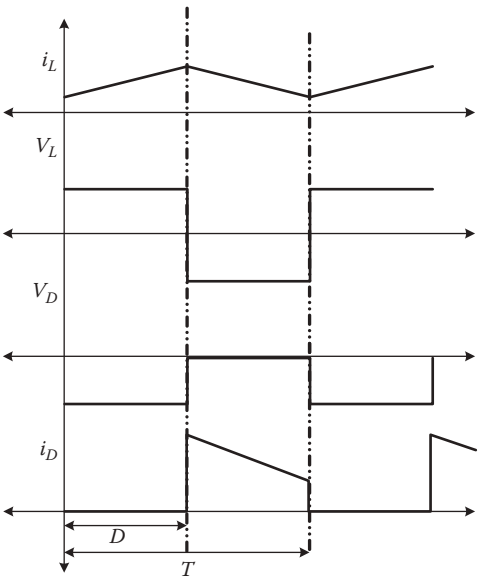


Figure 1.5 Operating mode waveforms of buck converter in CCM.

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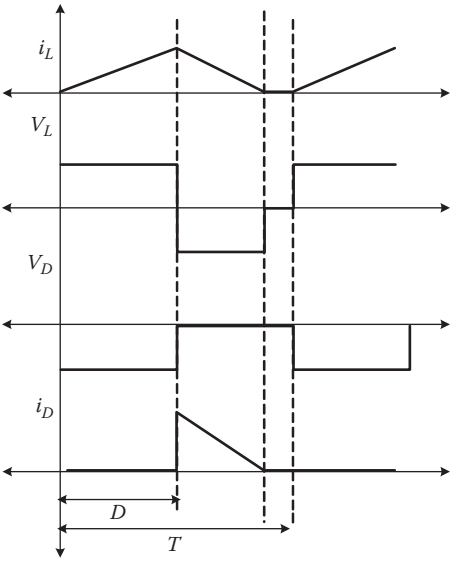


Figure 1.6 Operating mode waveforms of buck converter in DCM.

$$\frac{di_L}{dt} = \frac{V_d - V_o}{L} \tag{1.3}$$

$$i_L(t) = \frac{V_d - V_o}{L} t + I_{L,\min} \tag{1.4}$$

$$i_L(t = DT) = I_{L,\max} \tag{1.5}$$

$$I_L = I_{L,\max.} - I_{L,\min.} = \frac{V_d - V_o}{L} DT \tag{1.6}$$

Now for the second sub-interval,

$$DT < t < T \tag{1.7}$$

$$v_L = -V_o \tag{1.8}$$

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$$\frac{di_L}{dt} = \frac{-V_o}{L} \tag{1.9}$$

$$i_L(t) = \frac{-V_o}{L}(t - DT) + I_{L,\max} \tag{1.10}$$

$$i_L(t = T) = I_{L,\min} \tag{1.11}$$

$$I_L = I_{L,\max.} - I_{L,\min.} = \frac{V_o}{L}(1 - D)T \tag{1.12}$$

Equating to equations for I_L we can get,

$$\frac{V_d - V_o}{L} DT = \frac{V_o}{L}(1 - D)T \tag{1.13}$$

$$V_o = DV_d \text{ where } D = \frac{t_{on}}{T} \tag{1.14}$$

Thus, a buck converter is a step-down type, where the output voltage is always lower than the input. If it is assumed that the converter is in critical continuous/discontinuous conduction mode, minimum inductor current is zero, and thus I_L will become,

$$I_L = \frac{V_o}{L}(1 - D)T = \frac{V_o}{L}\left(1 - \frac{V_o}{V_d}\right)T \tag{1.15}$$

From this equation, we can write,

$$I_L = I_o = \frac{V_o}{R} \tag{1.16}$$

Equating the minimum inductor current equation to zero, we get,

$$I_L = \frac{V_o}{L}(1 - D)T = \frac{V_o}{L}\left(1 - \frac{V_o}{V_d}\right)T \tag{1.17}$$

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$$I_{L,\min.} = 0 \qquad \frac{1}{R} - \frac{(V_d - V_o)}{2LfV_d} = 0 \tag{1.18}$$

$$L = \frac{(V_d - V_o)R}{2fV_d} = \frac{(1-D)R}{2f} \tag{1.19}$$

This is the minimum inductance required to maintain the continuous conduction mode in the buck converter. Thus, if one needs to operate the buck converter in DCM, the value of the inductance should be less than this, given the specifications, for example, load, input-output voltage, and switching frequency.

Now let us consider the capacitor. From the operation of the converter, the capacitor is charged during the switch on period and discharged during the off sub-interval. Putting this in mathematical form it can be written as,

$$i_L = i_c + i_o$$

$$i_c \cong i_L - I_o = i_L - \frac{V_o}{R} \tag{1.20}$$

$$i_c = C\frac{dv_o}{dt} \tag{1.21}$$

Integrating the equation for capacitor current shown above for change in output voltage dV, the equation becomes,

$$i_c = C\frac{dv_o}{dt} \tag{1.22}$$

$$V_o = \frac{1}{C}\int_{t_1}^{t_2} i_c\,dt = \frac{1}{C} \quad Q = \frac{1}{C}\frac{1}{2}\frac{T}{2}\frac{I_L}{2} \tag{1.23}$$

Now, if the value of I_L is substituted in these equations from the equations shown before, the resulting equation will be,

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$$V_o = \frac{1}{8Cf} \frac{V_o}{L}(1-D)T \tag{1.24}$$

$$V_o = \frac{(1-D)V_o}{8LCf^2} \tag{1.25}$$

$$\frac{V_o}{V_o} = \frac{(1-D)}{8LCf^2} \tag{1.26}$$

$$C = \frac{(1-D)}{8L \quad V_O / V_O f^2} \tag{1.27}$$

This is the value of the capacitance for ripple voltage of V_O / V_O.

The switch should be selected to handle the maximum of the inductor current and it should handle the input voltage. The diode should be selected for load current and input voltage.

Output voltage regulation is provided by varying the duty cycle of the switch. The LC arrangement provides very effective filtering of the inductor current. Hence, the buck and its derivatives all have very low output ripple characteristics. The buck is normally operated in continuous mode where peak currents are lower; the smoothing capacitor requirements are smaller. There are no major control problems with the continuous mode buck. The conventional proportional-integral (PI) controller for the buck converter is shown in Figure 1.7.

1.2 Boost Converter

Operation of the boost converter is more complex than the buck operation. When the switch is on, diode D is reverse biased, and V_{in} is applied across inductor L. Current builds up in the inductor to a peak value, either from zero current in the discontinuous mode or an initial value in the continuous mode. When the switch turns off, the voltage across L reverses, causing the voltage at the diode to rise above the input voltage. The diode then conducts the energy stored in the inductor, plus energy direct from the supply to the smoothing capacitor and load. Hence, V_o is always greater than V_{in}, making this a step-up converter [5]. The power stage circuit is shown in the Figure 1.8. For continuous mode operation,

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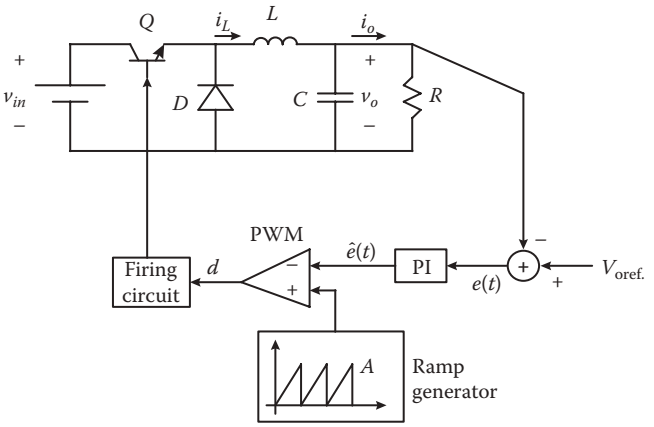


Figure 1.7 Conventional PI controller for buck converter.

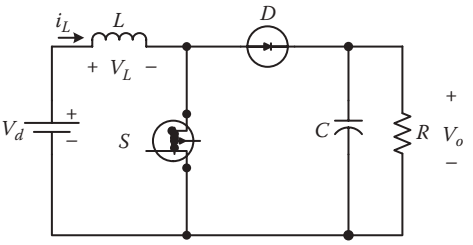


Figure 1.8 Boost converter.

the boost DC equation is obtained by a similar process as for the buck, and is given below:

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{1.28}$$

Similar to the buck converter, here also the state of the inductor current decides the operating mode. The converter can be operated in CCM as well as DCM. Both of these modes are examined in the following sections.

1.2.1 Boost Converter Operation in Continuous Conduction Mode

As the converter operation is to be examined in continuous mode, it is assumed that before the switch is on, there is some minimum current

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flowing through the inductor. As soon as the switch is on, the first sub-interval starts. The inductor current starts increasing linearly. The negative voltage across the diode forces it to be off. Thus, there is no current through the diode and the load is supplied entirely by the output capacitor. The power stage circuit is shown in Figure 1.9.

The inductor current goes on increasing linearly unless the switch is off. When the switch is off, the second sub-interval starts. The inductor has to deplete its energy once the switch is made off and this forces the diode to conduct. The diode starts conducting and some of the inductor energy supplies the load and some charges the capacitor. The power stage circuit for the sub-interval is shown in Figure 1.10.

The inductor current continues to decrease until the switch is made on again or it reaches zero. But here it is assumed that the converter operates in continuous conduction mode and thus, before the inductor current reaches zero, the switch is made on again. Once again the current starts increasing and the cycle repeats. The operating mode waveforms of the boost converter in continuous conduction mode are shown in Figure 1.11.

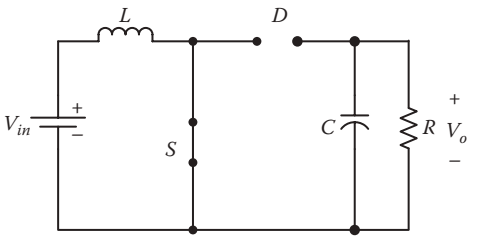


Figure 1.9 Boost converter when switch S is on.

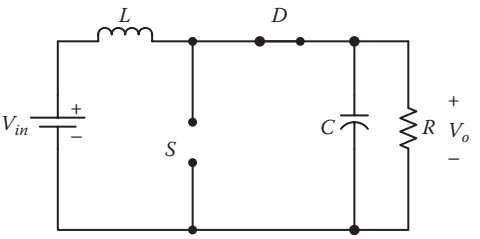


Figure 1.10 Boost converter when switch is off.

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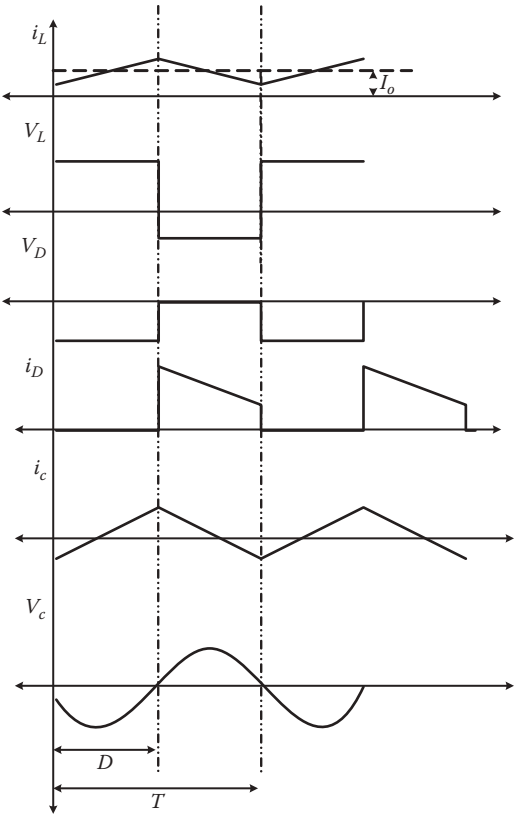


Figure 1.11 Operating mode waveforms for boost converter in CCM.

1.2.2 *Boost Converter Operating in Discontinuous Conduction Mode*

Here, also similar to the buck converter, the boost converter is said to be in discontinuous mode when inductor current reaches zero and stays zero. The first two sub-intervals of this operating mode are the same as those of the CCM [6]. In the second sub-interval, inductor current decreases. But here the switch is not turned on before current reaches zero. And thus, the current goes to zero, the third sub-interval starts and the current tries to become negative, but the diode will not allow the current in the opposite direction. Thus, the current stays at zero for some definite time unless the switch goes to on. The power stage circuit for this third sub-interval is shown in Figure 1.12.

Once the switch is on again, the current starts increasing from zero and this sub-interval ends. The cycle repeats itself. The operating mode

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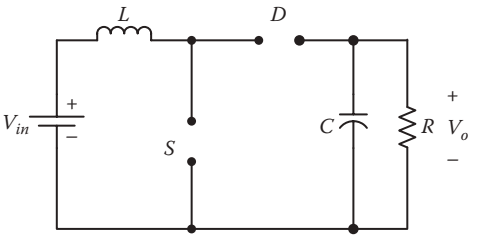


Figure 1.12 Boost converter when both switch S and diode D are off.

waveforms for the DCM operation are the same as those for the DCM of the buck converter.

1.2.3 Design Considerations for Boost Converter

Similar to the buck converter, the boost converter involves a switch, a diode, an inductor, and a capacitor. The switch and diode are to be designed depending on voltage and current stress they must handle for all possible operating conditions. The inductor must be designed to operate the converter in proper operating mode. The capacitor should meet the output voltage ripple requirement.

The switch has to sustain input voltage under extreme conditions and the maximum current that it has to handle is about twice the load current. The same can be applied to the diode for a worst-case scenario. If steady-state equations for inductor current and capacitor voltage are solved for each operating mode, for example, CCM, CCCM, and DCM as for the buck converter, it is possible to obtain design equations for the inductor and the capacitor. The value of inductance is given by,

$$L = \frac{RD(1-D)^2}{2f} \tag{1.29}$$

where L is the inductance of the inductor, R is the load resistance, D is duty ratio, and f is switching frequency. This is the value of inductance, which is needed to operate the converter in continuous conduction mode under all line-load conditions. The capacitance of the capacitor is given by,

$$C = \frac{D}{Rf \quad V_o / V_o} \tag{1.30}$$

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where C is the minimum value of capacitance of the output capacitor, to limit the output voltage ripple below V_O / V_O. D is duty ratio, R is load resistance, and f is switching frequency.

Again, in the boost converter, by controlling the duty cycle output regulation is achieved. From the boost waveform, the current of diode D is always discontinuous. Therefore, the output capacitor must be large, with a low equivalent series resistance (ESR) to produce a relatively acceptable output ripple. On the other hand, the boost input current is the continuous inductor current, and this provides low input ripple characteristics. The boost is very popular for capacitive load applications such as photoflashers and battery chargers.

If the boost is used in discontinuous mode, the peak transistor and diode currents will be higher, and the output capacitor will need to double in size to achieve the same output ripple as in continuous mode. In the discontinuous mode, the energy in the inductor at the start of each cycle is zero. This removes the inductance from the small signal response, leaving only output capacitance effect. This produces a much a simpler response, which is far easier to compensate and control.

1.3 Buck-Boost Converter

The buck-boost is also a member of the DC-DC converter family used extensively for advanced switching power supplies. The power stage of the topology is shown in Figure 1.13. When the switch is on, the diode is reverse biased and the input is connected across the inductor, which stores energy as previously explained. At turn-off, the inductor voltage reverses and the stored energy is then passed to the capacitor and load through the forward biased rectifier diode. There is a polarity inversion; the output voltage generated is negative with respect to input. The continuous mode DC equation is below:

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{1.31}$$

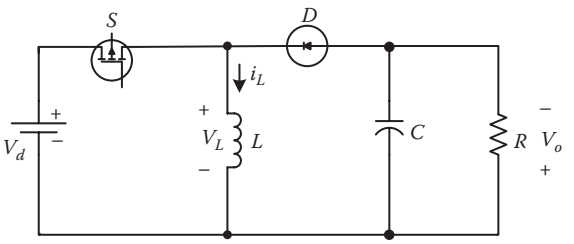


Figure 1.13 Buck-boost converter.

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D can be selected such that the output voltage can either be higher or lower than the input voltage. This gives the converter the flexibility to either step up or step down the supply [7]-[9]. Since both input and output currents are pulsating, low ripple levels are very difficult to achieve using the buck-boost. Very large output filter capacitors are needed—typically up to eight times that of a buck converter. The transistor switch also needs to be able to conduct the high peak current, as well as supporting the higher summed voltage.

Though the polarity of the output voltage is not similar to the input voltage, unlike the buck and boost converters, the buck-boost converter can handle similar operating modes, for example, continuous or discontinuous conduction modes. Both of these modes are explained in the following sections.

1.3.1 Buck-Boost Converter in Continuous Conduction Mode

As the converter is assumed to be operating in continuous conduction mode, the inductor current has some definite minimum value before time t = 0, for example, before the switch is on. As soon as the switch is on, the first sub-interval of the switching period starts. The inductor current starts increasing from its minimum value. The diode is reverse biased and thus off. The output capacitor supplies the load in this sub-interval and therefore it is discharged, too. The power stage appears as shown in Figure 1.14. The decrease in capacitor voltage is also linear.

The inductor current keeps on increasing until the switch is made off. The off command can be from pulse-width modulation (PWM), pulse-frequency modulation (PFM), or any other kind of controller. Once the switch is made off the first sub-interval ends and the second one starts. In the second sub-interval, the inductor depletes the energy partly through the output capacitor and partly through the load. Thus, the inductor current decreases linearly in this sub-interval and the capacitor charge increases linearly. The diode is on in this interval and allows the inductor current to flow thorough it. The power stage circuit for this sub-interval is shown in Figure 1.15.

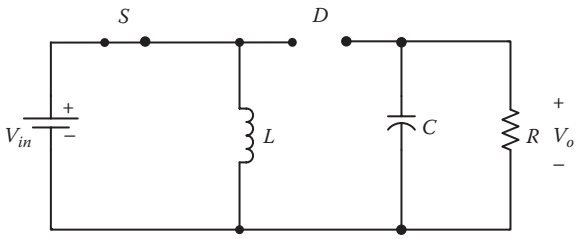


Figure 1.14 Buck-boost converter when switch S is on.

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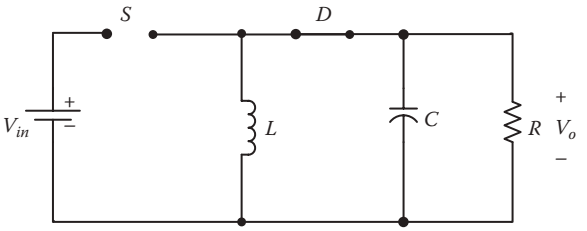


Figure 1.15 Buck-boost converter when switch is off and diode is on.

The inductor current decreases unless it reaches zero or the switch is turned on again. As converter operation is examined in continuous conduction mode, the inductor current cannot go to zero, and thus before it goes to zero the switch is turned on again, the inductor current again starts increasing and the cycle continues. The operating mode waveforms of the buck-boost converter in continuous conduction mode are shown in Figure 1.16.

1.3.2 Buck-Boost Converter in Discontinuous Conduction Mode

Similar to the other converters, for the buck-boost converter in discontinuous conduction mode the first two sub-intervals remain the same. The DCM operation includes a third sub-interval. The second sub-interval continues until the switch current keeps decreasing and does not reach zero. As soon as the inductor current reaches zero, the third sub-interval starts. The inductor current tries to be negative but the diode cannot

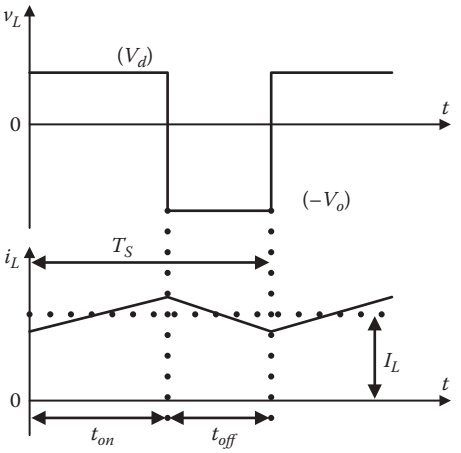


Figure 1.16 Operating mode waveforms of buck-boost converter in CCM.

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conduct in the opposite direction, and thus the current stays zero. The capacitor voltage also remains at its initial position, for example, constant. The sub-interval comes to an end when the switch goes off. The power stage in the third sub-interval will appear as shown in Figure 1.17.

Once the switch is made on, the inductor current starts increasing from zero. Here it must be noted that the switch is always on after the inductor current reaches zero, not before that, and therefore the inductor current has zero initial value. The operating mode waveforms in DCM are shown in Figure 1.18.

1.3.3 Design Considerations for Buck-Boost Converter

Similar to the previous two converters, for example, buck and boost, this converter has one switch, one diode, one inductor, and one capacitor design. The design criteria for all the components remain the same as those for previous converters. The design procedure also remains the same, thus it is not discussed here. The result of the mathematical analysis of every operating mode and solutions of the equations for inductor current are given here:

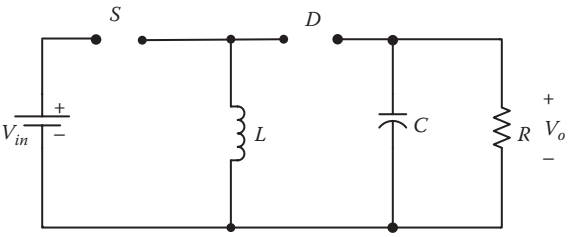


Figure 1.17 Buck-boost converter when both switch S and diode D are off.

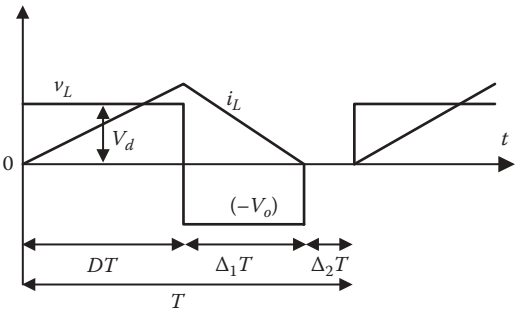


Figure 1.18 Operating mode waveforms of buck-boost converter in DCM.

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$$L = \frac{R(1-D)^2}{2f}, \tag{1.32}$$

where L is the value of the inductance of the inductor, R is the load impedance, D is duty ratio, and f is switching frequency. An inductance value more than the equation given above will force the converter to operate in continuous conduction mode. And a value less than that will result in converter operation in discontinuous conduction mode. The capacitance value is given by,

$$C = \frac{D}{Rf \quad V_o / V_o}, \tag{1.33}$$

where C is the minimum value of the capacitance, in farads, required to limit the output voltage ripple lower than V_O / V_O, generally given in percentage value. D is the duty ratio for the switch, R is the load impedance in ohms, and f is the switching frequency, generally in kHz. The switch must be selected for maximum input voltage and maximum inductor current, while the diode must handle load current and load voltage.

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chapter two

Isolated DC-DC Converters

Most power supplies and power electronics circuitries are designed to meet some or all of the following requirements [1]-[5]:

1. Electrical isolation: The primary advantage of electrical isolation is that the input and output are not electrically connected. If the input supply is ground, the same ground will not be present at output. The transformers utilized in these structures provide two important functions. One is to provide isolation. The other is to step down or step up the time-varying voltages and currents. In addition, by utilizing a very high switching frequency the size of the transformer can be minimized.
2. Regulated output.
3. Multiple outputs provide the possibility of feeding different loads simultaneously.

This chapter addresses the most common isolated DC-DC converters such as full-bridge, half-bridge, flyback, forward, and push-pull, and their operational principles. The full-bridge converter and half-bridge converter are derived from the step-down converter. Flyback converters are derived from the buck-boost converters. Forward converters and push-pull converters are derived from the step-down converters with isolation.

There are two kinds of core excitation for the above converters. One is the unidirectional core excitation, where only the positive part (quadrant I) of the B-H loop is used (flyback and forward converters). The other is the bidirectional core excitation, where the positive (quadrant I) and the negative (quadrant III) parts of the B-H loop are utilized alternatively (push-pull, half-bridge, and full-bridge converters). The whole system construction is shown in Figure 2.1.

2.1 Flyback Converter

The topology of a flyback converter is presented in Figure 2.2. The use of a single transistor switch means that the transformer can only be driven unipolarly [4]. This results in a large core size. The flyback, which is an isolated version of the buck-boost, does not contain a transformer, but utilizes a coupled inductor arrangement. When the transistor is turned on,

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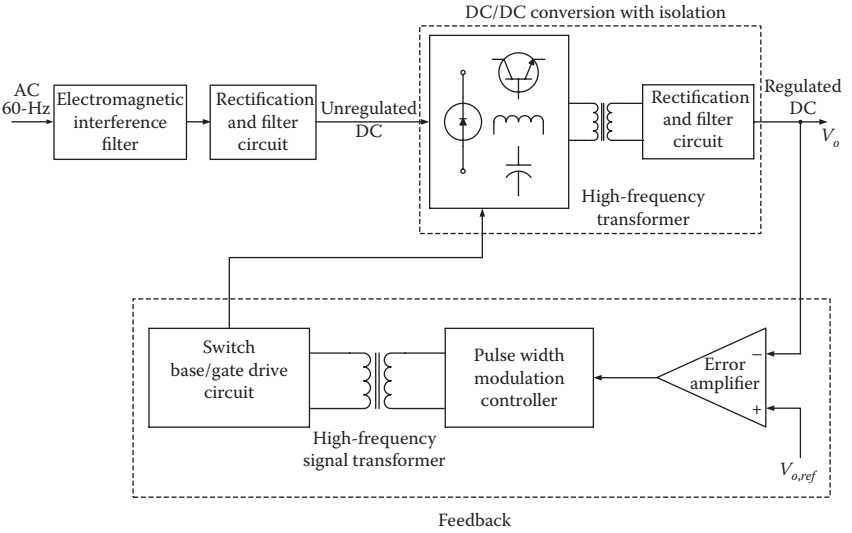


Figure 2.1 System construction for isolated converters.

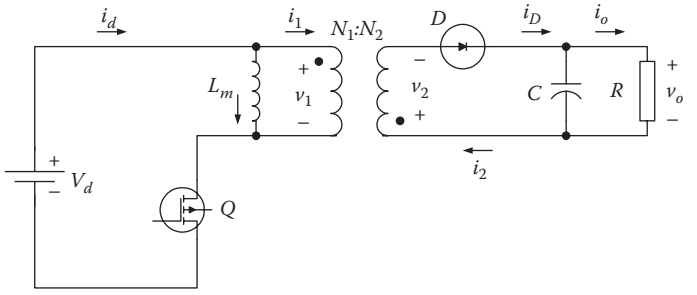


Figure 2.2 Flyback converter.

current builds up in the primary and energy is stored in the core; this energy is then released to the output circuit through the secondary when the switch is turned off. (A normal transformer such as the types used in the buck-derived topologies couples the energy directly during transistor on-time, ideally storing no energy.)

The fact that all of the output power of the flyback has to be stored in the core as 1/2LI^2 energy means that the core size and cost will be much greater than in the other topologies, where only the core excitation (magnetization) energy, which is normally small, is stored. This means that the transformer bulk is one of the major drawbacks of the flyback converter. In order to obtain sufficiently high stored energy, the flyback primary inductance

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has to be significantly lower than required for a true transformer, since high peak currents are needed. This is normally achieved by gapping the core. The gap reduces the inductance, and most of the high peak energy is then stored in the gap, thus avoiding transformer saturation (Figures 2.3 and 2.4).

The minimum inductor L_m and capacitor for flyback in CCM are decided by the following equations:

$$L_{m,\min.} = \frac{R(1-D)^2}{2f}\left(\frac{N_1}{N_2}\right)^2 \tag{2.1}$$

$$\frac{V_o}{V_o} = \frac{D}{RCf} \tag{2.2}$$

In the flyback converter, the secondary inductance is in series with the output diode when current is delivered to load. Hence, each output requires only one diode and output filter capacitor. Flyback is the ideal choice for generating low cost, multiple output supplies. Flyback is also ideal for generating high voltage outputs. However, there is a voltage spike at turn-off due to the stored energy in the transformer leakage inductance.

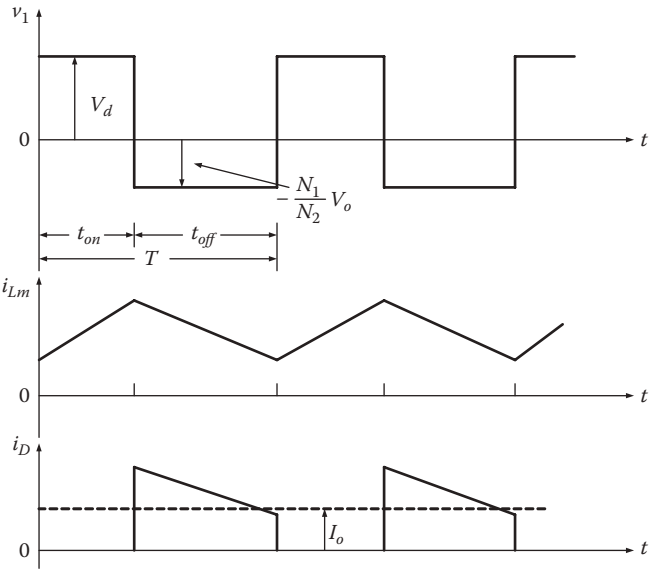


Figure 2.3 Waveforms of inductor and diode current in CCM.

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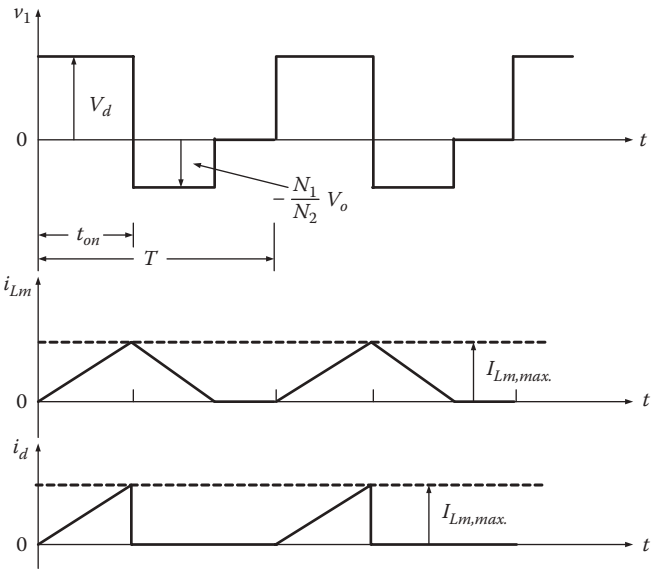


Figure 2.4 Waveforms of inductor and diode current in DCM.

The transistor must be capable of blocking approximately twice the supply voltage plus the leakage spike. Flyback converters have inherently much higher output ripples than other topologies. This, together with the higher peak currents, large capacitors, and transformer, limits the flyback to lower output power applications in the 20 to 200 W range.

2.2 *Forward Converter*

The topology of a forward converter is presented in Figure 2.5. The waveforms for the forward converter in CCM are shown in Figure 2.6.

The voltage ratio is

$$V_o = \frac{N_2}{N_1} D V_d \tag{2.3}$$

The minimum inductor L_m and capacitor for flyback in CCM are decided by the following equations:

$$L = \frac{(V_d - \frac{N_1}{N_2} V_o) R}{2 f V_d} = \frac{(1-D) R}{2 f} \tag{2.4}$$

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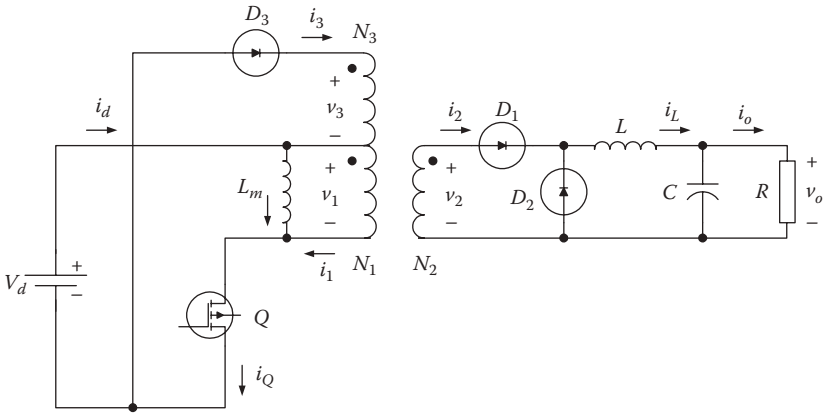


Figure 2.5 Forward converter.

$$\frac{V_o}{V_o} = \frac{1-D}{8LCf^2} \tag{2.5}$$

The forward converter is also a single-switch isolated topology. This is based on the buck converter. In contrast to the flyback, the forward converter has a true transformer action, where energy is transferred directly to the output through the inductor during the transistor on time. When the transistor turns off, the secondary voltage reverses, D1 goes from conducting to blocking mode, and the freewheel diode D2 then becomes forward biased and provides a path for the inductor current to continue to flow. This allows the energy stored in L to be released into the load during the transistor off time.

The forward converter is always operated in continuous mode, because this produces very low peak input and output currents and small ripple components. Since the transformer in this topology transfers energy directly, there is negligible stored energy in the core compared to the flyback. However, there is a small magnetization energy required to excite the core, allowing it to become an energy transfer medium. This energy is very small and only a very small primary magnetization current is needed. This means that a high primary inductance is usually suitable, with no need for the core air gap required in the flyback. Standard ungapped ferrite cores with high permeability are ideal for providing the high inductance required. Negligible energy storage means that the forward converter transformer is considerably smaller than the flyback, and core loss is also much smaller for the same throughput power.

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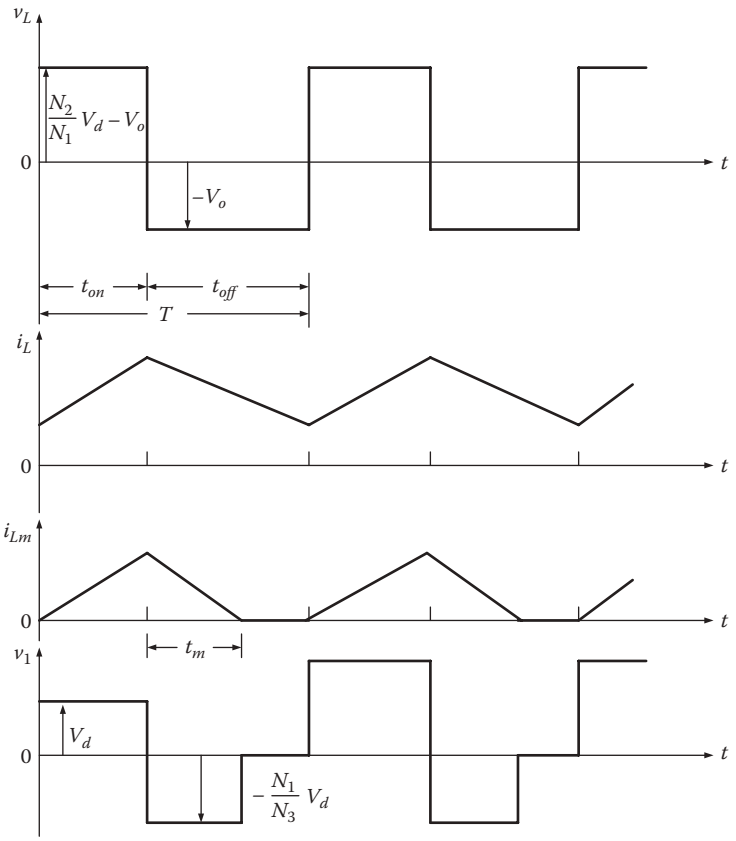


Figure 2.6 Circuit waveforms in CCM.

However, the transformer is still operated asymmetrically, which means that power is only transferred during the switch on time, and this poor utilization means the transformer is still far bigger than in the symmetrical types. In addition, a major problem is how to remove the core magnetization energy by the end of each switching cycle. This path is provided by adding an additional reset winding of opposite polarity to the primary. If this did not happen, there would be a net DC flux build-up, leading to core saturation and possible transistor destruction.

2.3 *Push-Pull Converter*

The primary concept of the push-pull converter (Figure 2.7) is a center-tapped arrangement and each transistor switch is driven alternately, driving the transformer in both directions. The push-pull transformer is

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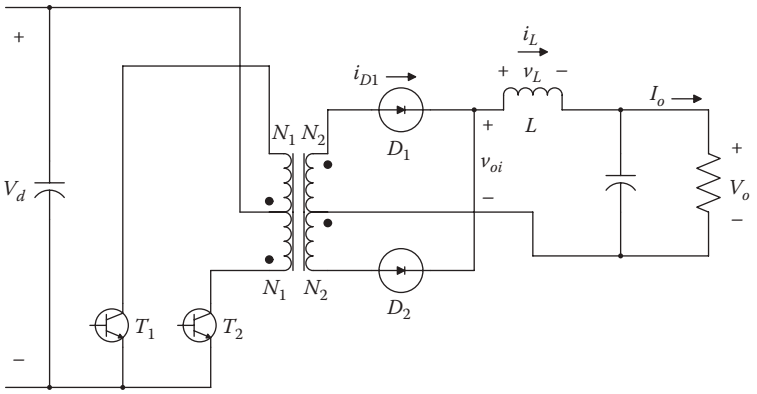


Figure 2.7 Push-pull converter.

typically half the size of that for the single-ended types, resulting in a more compact design. This push-pull action produces core resetting during each half cycle; hence, no clamp winding is required. Power is transferred to the buck type output circuit during each transistor conduction period. The push-pull configuration is normally used for output power in the 100 to 500 W ranges. Push-pull converters are thus excellent for high power density, low ripple output.

The push-pull offers very compact design of the transformer and output filter, while producing very low output ripple. So if space is a premium issue, the push-pull could be suitable. However, one of the main drawbacks of the push-pull converter is the fact that each transistor must block twice the input voltage due to the doubling effect of the center-tapped primary, even though two transistors are used.

A further problem with the push-pull is that it is prone to flux symmetry imbalance. If the flux swing in each half cycle is not exactly symmetrical, the volt-second will not balance and this will result in transformer saturation, particularly for high input voltage. Symmetry imbalance can be caused by different characteristics in the two transistors such as storage time in a bipolar and different on state losses.

The center-tape arrangement also means that extra copper is needed and very good coupling between the two halves is necessary to minimize possible leakage spikes. It should also be noted that if snubbers are used to protect the transistor, the design must be very precise since they tend to interact with each other. This is true for all symmetrically driven converters.

These advantages usually dictate that the push-pull is normally operated at lower voltage inputs such as 12, 28, or 48 V. DC-DC converters found in the automotive and telecommunication industries are often

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push-pull designs. At these voltage levels, transformer saturation is easier to avoid. Since the push-pull is commonly operated with low DC voltages, a selection guide for suitable power MOSFET is also included for 48 and 96 V applications.

The voltage ratio is:

$$V_o = 2\frac{N_2}{N_1}DV_d \tag{2.6}$$

The current waveforms for output inductor and diode D1 are shown in Figure 2.8.

2.4 Full-Bridge Converter

In the half-bridge converter, the maximum current rating of the power transistors will eventually determine the upper limit of the output power. The transistors are driven alternately in pairs: T_1 and T_3 simultaneously, and then T_2 and T_4. The transformer primary is now subjected to the full input voltage. The current levels flowing are halved compared to the half-bridge for a given power level. Hence, the full-bridges (Figure 2.9) will double the output power of the half-bridge using the same transistor types.

The secondary circuit operates in exactly the same manner as the push-pull and half-bridge, producing very low ripple outputs at very high current levels. Therefore, the waveforms for the full-bridge are identical

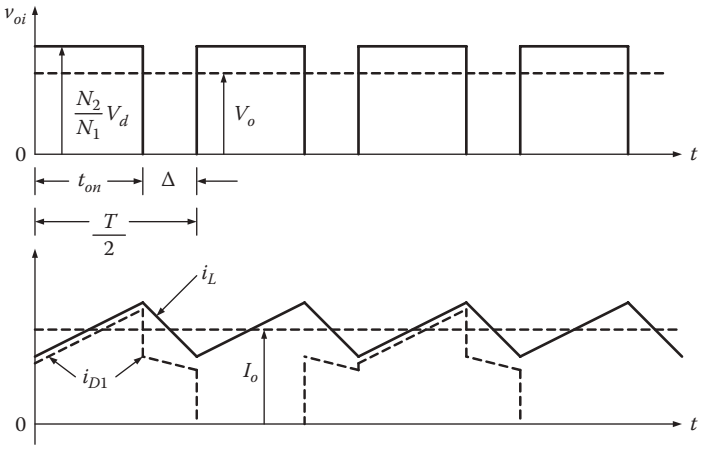


Figure 2.8 Current waveforms for output inductor and diode D1 for push-pull converter.

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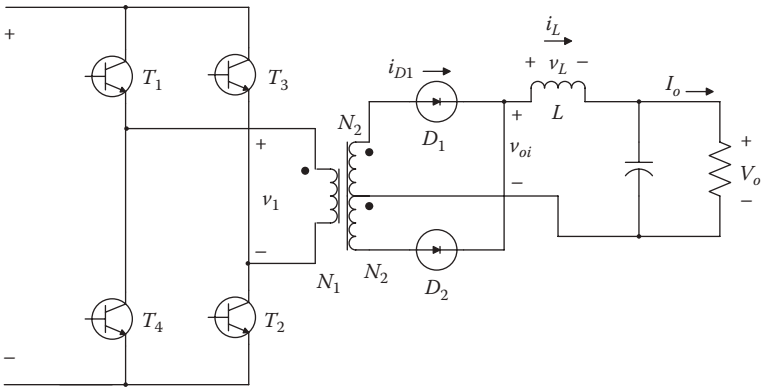


Figure 2.9 Full-bridge converter.

to the half-bridge waveforms, except for the voltage across the primary, which is effectively doubled.

The full-bridge is ideal for the generation of very high output power level. The increased circuit complexity normally means that the full-bridge is reserved for applications with power output level of 1 kW and above. For such high power requirements, designers often select Darlington power, since its superior current rating and switching characteristics provide additional performance and in many cases a more cost-effective design.

The full-bridge also has the advantage of only requiring one main smoothing capacitor compared to two for the half-bridge, hence saving space. Its other major advantages are the same as for the half-bridge.

However, four transistors and clamp diodes are needed instead of two for the other symmetrical types. An isolated drive for two floating potential transistors is now required. The full-bridge has the most complex and costly design of any of the converters discussed, and should only be used where other types do not meet the requirements. Again, the four transistor snubbers must be implemented carefully to prevent interactions occurring between them.

The voltage ratio is:

$$V_o = 2\frac{N_2}{N_1}DV_d \tag{2.7}$$

The current waveforms for output inductor and diode D1 are shown in Figure 2.10.

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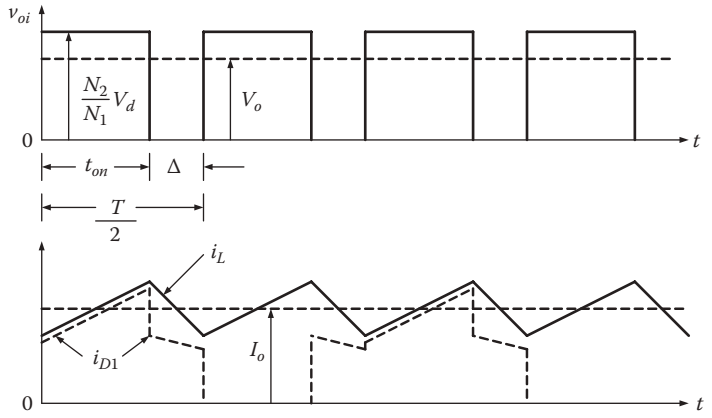


Figure 2.10 Current waveforms for output inductor and diode D1 for full-bridge converter.

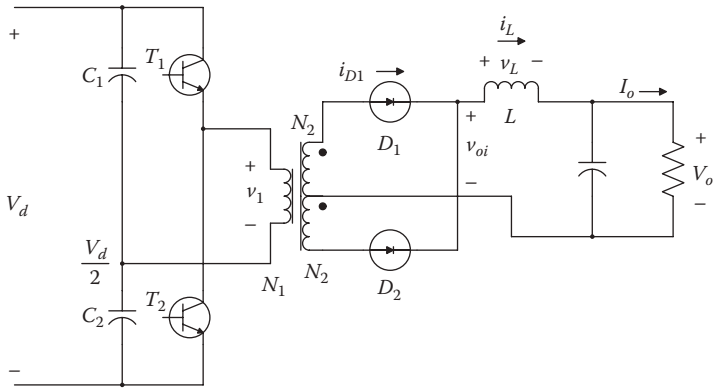


Figure 2.11 Half-bridge converter.

2.5 *Half-Bridge Converter*

The half-bridge converter (Figure 2.11) is also referred to as the single-ended push-pull, and in principle is a balanced version of the forward converter. Again it is a derivative of the buck type. The half-bridge has some key advantages over the push-pull, which usually makes it first choice for higher power applications in the 500 to 1000 W range.

As shown in Figure 2.11, the two main bulk capacitors C_1 and C_2 are connected in series, and an artificial input voltage mid-point is provided. The two transistor switches are driven alternately, and this

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connects each capacitor across the single primary winding each half cycle. $V_{in}/2$ is superimposed symmetrically across the primary in a push-pull manner. A full wave buck output filter rather than a half wave filter is implemented. This again results in very efficient core utilization. The waveforms are identical to the push-pull, except that the voltage across the transistor is halved.

This means that the half-bridge is particularly suited to high voltage inputs, such as off-line applications. Another major advantage over the push-pull is that the transformer saturation problems due to flux symmetry imbalance do not occur. By using a small capacitor, DC build-up of flux in the transformer is blocked, and only symmetrical AC is drawn from the input.

A less obvious exclusive advantage of the half-bridge is that the two series reservoir capacitors already exist, and this makes it ideal for implementing a voltage doubling circuit. This permits the use of either 110 or 220 V mains as selectable input to the supply.

The bridge circuits also have the same advantages over the single-ended types that the push-pull possesses, including excellent transformer utilization, very low output ripple, and high output power capabilities. The limiting factor in the maximum output power available from the half-bridge is the peak current handling capabilities of present day transistors. The upper power limit is typically 1000 W. For higher output powers the four-switch full-bridge is normally used.

However, the need for two 50 or 60 Hz input capacitors in the structure of the half-bridge is a drawback because of their large size. The top transistor must also have isolated drive, since the gate or base is at a floating potential. Furthermore, if snubbers are used across the power transistors, great care must be taken in their design because the symmetrical action means that they will interact with one another. The circuit cost and complexity have clearly increased and must be weighed against the advantage gained. In many cases, this normally excludes the use of the half-bridge at output power levels below 500 W.

The voltage ratio is:

$$V_o = 2\frac{N_2}{N_1} DV_d \tag{2.8}$$

The current waveforms for output inductor and diode D1 are shown in Figure 2.12.

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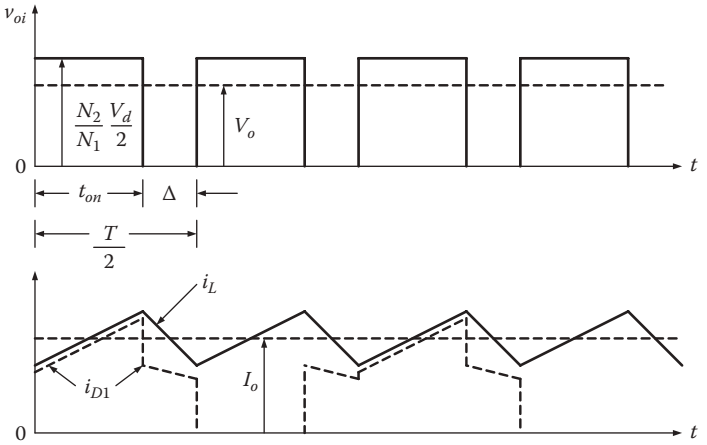


Figure 2.12 Current waveforms for output inductor and diode D1 for half-bridge converter.

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chapter three

Power Factor Correction

Electronic equipment connected to main components interact with the supply grid to a varying extent. Passive loads such as resistive heaters draw current linearly and do not affect the operation of other equipment connected to the same mains. Most power electronic devices switch the current on and off rapidly and this causes disturbances in the main network in the form of additional current harmonics. These harmonics are generated by the switching action in the equipment and may interfere with sensitive electronic devices connected to the same network. Legislation has been introduced that specifies acceptable levels of reflected harmonics from power electronic equipment into the mains. Utility companies do not like this switching behavior because it causes them to supply extra power to the equipment and install extra thick cabling to account for circulating current. Some of the power electronic topologies, mainly DC-DC converters, offer the characteristic of making any switching load appear as resistive load. In other words, these controllers draw the line current proportional to the line voltage. This chapter discusses various power electronic converters for power factor correction and special converters used for motor drives to achieve good power factor.

Generally, mains-connected power supplies consist of a bridge rectifier followed by a DC link capacitor. The DC-DC regulator is supplied from this DC link capacitor. The DC link capacitor is used to make the voltage constant, which goes into the DC-DC converter stage. The capacitor draws current from the mains only when the instantaneous mains voltage is greater than the capacitor voltage. Since the capacitor is chosen for a certain hold-up time, if its time constant is much greater than the frequency of the mains, the mains should miss a number of cycles. This implies that the instantaneous mains voltage is greater than the capacitor voltage only for very short periods of time (charging time of capacitor). During this short period the capacitor must charge fully. Therefore, large pulses of current are drawn from the line over a very short time. This is true for most of the rectified AC signals with capacitive filtering.

3.1 Concept of PFC

PFC is an abbreviation for power factor correction. Any electrical system can be simplified as shown in Figure 3.1.

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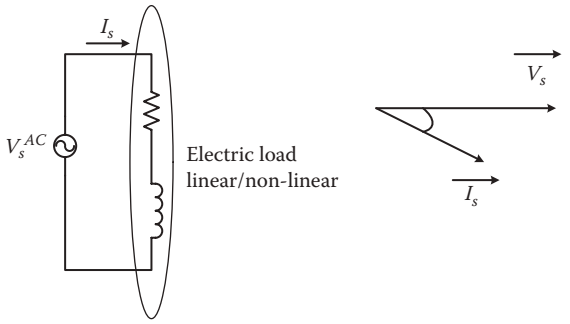


Figure 3.1 Generalized electrical system block diagram.

Depending on the loading on the utility, the current shape will be different. The load can be linear, such as in resistive heaters, or it can be nonlinear, such as in an advanced air conditioner with switching power supply. Figure 3.2 shows the effect of load on the line current wave shape, and thus the effect on power quality.

If the load is linear the supply voltage and current waveforms are sinusoidal as given in Figure 3.2 and the power factor is given by

$$COS\,\Phi = \frac{V_S}{I_S} \tag{3.1}$$

though advance loads consist of advance switching power supplies in them. As mentioned in the first section of the chapter, mostly these switching power supplies have diode rectifiers on their front ends. The current waveforms are no longer sinusoidal for them, and thus the definition of power factor is changed for them. It is given by

$$\text{PF} = \frac{\text{DPF}}{\sqrt{1 + THD^2}} \tag{3.2}$$

where DPF is displacement power factor and THD is total harmonic distortion. Definition of both is given by



Figure 3.2 Supply voltage and current for (left) linear and (right) non-linear load.

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$$\text{DPF} = \cos \Phi_1 = \frac{V_S}{I_{S1}}$$

where I_{S1} is fundamental component of the supply current,

$$THD = \frac{I_{distortion}}{I_{S1}} \tag{3.3}$$

Generally nonlinear loads, such as power electronic equipped supplies, cause following problems:

- Creation of harmonics and electromagnetic interference (EMI)
- High losses
- Requirement of over-dimensioning of parts
- Reduced maximum power capability from the line

Power factor corrector makes the load look more like a resistive element than a nonlinear one without PFC. Modern PFC circuits can achieve power factor very near to unity (for example, >0.99). PFC circuits have following advantages:

- Better source efficiency
- Overall lower power installation cost
- Lower conducted EMI
- Reduced peak current levels
- Ability to act as filter for conducted EMI
- Common input filter for paralleled supplies
- Better chance of agency approval

However, PFC circuits have one or more of the following disadvantages:

- Introducing greater complexity into the design.
- Having more parts adversely affects reliability.
- The generation of EMI and radio frequency interference (RFI) by the active PFC circuits requires extra filtering, making the input filter more complex and more expensive.
- More parts require a more costly power solution.
- Higher utility cost.

Harmonic standards developed by the Institute of Electrical and Electronics Engineers (IEEE) and the International Electrotechnical Commission (IEC) are enforced in many parts of the world including

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Europe. Although they are not enforced in the United States, they have attracted a lot of attention in the power electronics industry. In most applications it is not difficult to meet these standards; however, the most economic choices are still being developed. IEEE and international harmonic standards can be grouped into three main categories:

1. Customer system limits
   - IEEE 519-1992
   - IEC 1000-3-2 (compatibility levels)
   - IEC 1000-3-6
2. Equipment limits
   - IEC 1000-3-2
   - IEC 1000-3-4
   - New task force in IEEE (harmonic limits for single phase loads)
3. How to measure harmonics
   - IEC 1000-4-7

A summary of a few of the above regulations in terms of harmonic current limitations are given in Tables 3.1 and 3.2. The IEC 1000 series deals with electromagnetic compliance. Part 3 sets limits and series 2 limits har-

Table 3.1 IEC 1000-3-2 Limits for Class-D Equipment

Harmonic Order (n)	Maximum Permissible Harmonic Current per Watt (mA/W)	Maximum Permissible Harmonic Current (A)
3	3.40	2.30
5	1.90	1.14
7	1.00	0.77
9	0.50	0.40
11	0.35	0.33

Table 3.2 IEC 1000-3-4 Harmonic Limitation

Minimal R_{SCC}	Upper Limits for Harmonic Distortion Factors		Limits for Individual Harmonics in % of I_1			
	THD	PWHD	I_5	I_7	I_{11}	I_{13}
66	17	22	12	10	9	6
120	18	29	15	12	12	8
175	25	33	20	14	12	8
250	35	39	30	18	13	8
350	48	46	40	25	15	10
450	58	51	50	35	20	15

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monic current emissions for equipment input current less than or equal to 16 A.

IEC 1000-3-4 not only deals with individual equipment but also sets limits for the whole system installation. Both single-phase and three-phase harmonic limits are addressed in this section of the regulation.

On the other hand, IEEE standard 519 sets limits of harmonic voltage and current at the point of common coupling (PCC). The philosophy behind this standard is to prevent harmonic currents from traveling back to the power system and affecting other customers. Tables 3.3 and 3.4 list the IEEE-519 voltage harmonic and current harmonic limits.

3.2 General Classification of PFC Circuits

Depending on the position of the PFC circuit, it can be classified into two major categories. The first is input PFC and the second is output PFC. Input PFC means a system in which the power factor correction circuit is placed at the input of the offending network, such as switched-mode power supply (SMPS). When loads are highly reactive, for example, ballasts, the PFC circuit is placed between this kind of load and the power supply. This circuit is known as output PFC.

Depending on the components used to develop the PFC circuits, they can also be classified in two ways. The first is passive PFC circuits and the second is active PFC circuits. When simple reactive components, such as inductors and capacitors, are used to correct the displacement between line voltage and line current, the process is known as passive PFC. To

Table 3.3 IEEE 519 Voltage Harmonic Limits

Bus Voltage (kV)	Maximum Individual Harmonic Component (%)	Maximum THD (%)
69 and below	3.0	5.0
115 to 161	1.5	2.5
Above 161	1.0	1.5

Table 3.4 IEEE 519 Current Harmonic Limits

SCR	H<11	11–16	17–22	23–34	35<	THD
<20	4	2.0	1.5	0.6	0.3	5
20–50	7	3.5	2.5	1.0	0.5	8
50–100	10	4.5	4.0	1.5	0.7	12
100–1000	12	5.5	5.0	2.0	1.0	15
>1000	15	7.0	6.0	2.5	1.4	20

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solve the problem of poor power factor, and thus total harmonic distortion, switching converters with active control circuits are employed as active PFC. Both of them have their relative merits and demerits.

Active PFC circuits are generally used to compensate for distortion of the mains current. These circuits are mostly switched-mode power supply topologies. This means that they are more complicated than passive circuits. With the advancements in integrated circuit (IC) technology, they are becoming simpler, more compact, and also less costly. These power electronic topologies are able to achieve power factor of more than 99% and THD less than 5%. From the operating frequency point of view, they can be either slow switching topologies or high switching topologies. Next, we discuss high switching topologies in detail.

3.3 High Switching Frequency Topologies for PFC

High frequency PFC topologies are the most common of all PFC circuits. They are supported by control ICs from most of the major manufacturers. High frequency circuits offer many advantages over passive and low frequency techniques. Such advantages are low weight, accurate voltage control, low line harmonic distortion, wide operating voltage range, and easy design.

The pre-regulator can be any one of the basic DC-DC converter topologies, for example, buck, boost, buck-boost, Ćuk, flyback, forward, SEPIC, and zeta. Their performance characteristics, block diagrams, suitability to the application, and relative advantages and disadvantages are discussed in the following subsections. The pre-regulators are designed to draw an input current, which varies in direct proportion to the instantaneous input voltage. The control circuits control the root mean square (RMS) current drawn from the line. Though the circuits are more complex, power factor of almost unity is achievable with these high frequency topologies. All the topologies can operate in both discontinuous conduction mode (DCM) as well as in continuous conduction mode (CCM) mode. Most of the PFC topologies provide power factor correction in DCM, and thus in this section converters are considered as operating in DCM, unless specified.

3.3.1 Buck Converter as Power Factor Corrector

For the buck converter the output voltage is always less than the peak input voltage (Table 3.5). Power factor correction is therefore not achieved when the instantaneous input voltage is lower than the required output voltage [1]. This topology, on its own, is not suitable for PFC. Improved performance is obtained if cascaded with a boost circuit. By doing so the current can be limited to the boost circuits, which is not possible with

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Table 3.5 Parameters of PFC Buck Converter

Parameter	Value
Input voltage, V_{in}	110
Switching frequency, f_s	50 k
Output voltage, V_{out}	10
Inductance, L	100 u

boost topology alone. The buck topology has a switch in series with the mains or supply line. Thus, the input current is switched directly, which in turn can generate EMI problems. The drive circuit for the switch is more complex than that for the boost circuit. The advantages with buck can be summarized as follows: less stress on the bulk capacitor, voltage rating of the switch is much less than the boost one (for the same power rating of the converter), and inrush current protection is inherent [2]. Disadvantages are that the power factor cannot be achieved when input voltage is less than output voltage, power factor cannot be achieved as good as 98% unless it is used with a boost pre-regulator, and a large input filter is required to reduce THD and floating drive circuits (Figures 3.3 and 3.4).

3.3.2 Boost Converter as Power Factor Corrector

This pre-regulator is the most popular for PFC [3]. The DC-link capacitor after the diode bridge is usually set at the voltage about 10% greater than the peak input voltage. It must be noted that if the peak input voltage exceeds the controlled capacitor voltage then power factor correction is not achieved (Table 3.6). The input current from the mains is not chopped directly in this topology, because the inductor is placed in series with the source. And this helps with EMI, but care must be taken with the high frequency current that is drawn from the line. Fortunately, the series choke at the input of the PFC circuit helps to absorb some of the line transients. The voltage across the switch is only the output voltage–low voltage source on the switch. Finally, the emitter or source of the switch is referenced to zero voltages and this makes the drive circuit simpler than the other

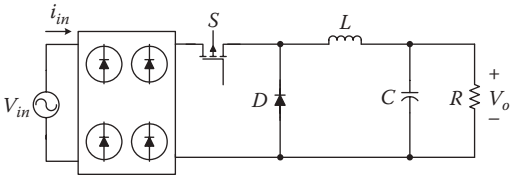


Figure 3.3 PFC buck converter.

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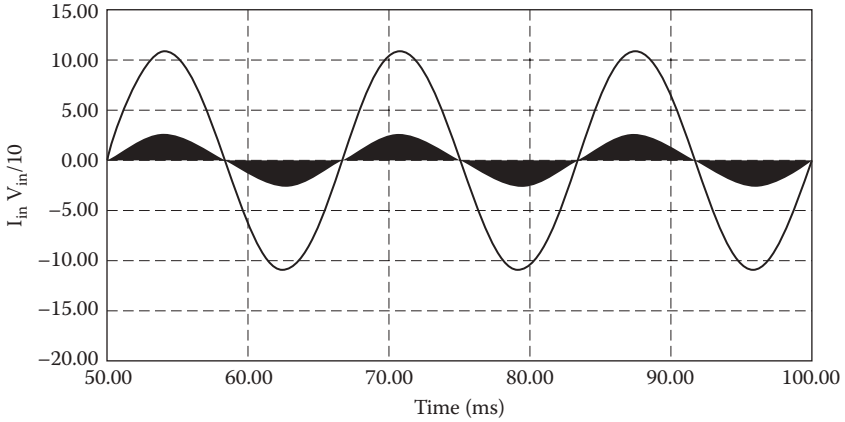


Figure 3.4 Input voltage and current with buck converter as PFC.

Table 3.6 Parameters for PFC Boost Converter

Parameter	Value
Input voltage, V_{in}	110
Switching frequency, f_s	50 k
Output voltage, V_{out}	10
Inductance, L	100 u
Capacitance, C	500 u

topologies. This method does not offer inrush current limiting as the input inductor is comparatively small, so this must be accomplished by other means. The advantages of the boost converter can be summarized as follows: good EMI performance, voltage rating of the switch is a bit less than other topologies, it absorbs line transients, and easy drive circuits are required. On the negative side, it offers no PFC control when input voltage is higher than the output voltage, and it cannot limit the inrush currents (Figures 3.5 and 3.6) [4].

3.3.3 Buck-Boost Converter as PFC

In this topology, current that the converter draws from the grid is linearly proportional to the input voltage. So we can say that input current follows the input voltage [5], [6]. At the same time the output voltage is allowed to vary independently in a specified range (Table 3.7). These two features make this topology most suitable for the application where a

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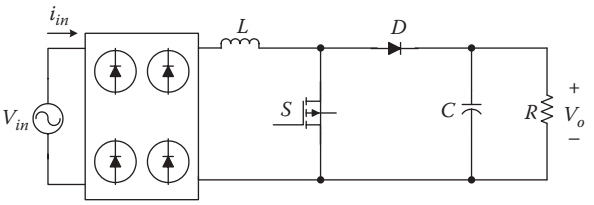


Figure 3.5 PFC boost converter.

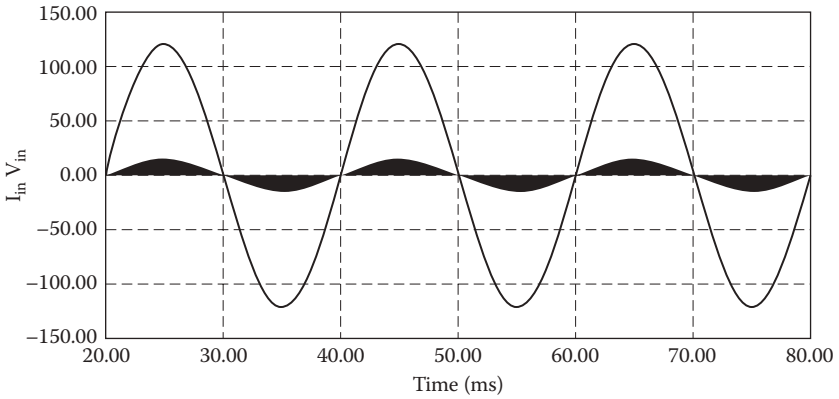


Figure 3.6 Input voltage and current for boost converter as PFC.

Table 3.7 Buck-Boost Converter

Parameter	Value
Input voltage, V_{in}	110
Switching frequency, f_s	50 k
Output voltage, V_{out}	30
Inductance, L	75 u
Capacitance, C	470 u

wide range of output voltage is necessary. But this topology too has limitations. One of them is that the polarity of its output voltage is reversed. This means that the input and output should have separate grounds. And the other limitation is that the drive circuit for this topology is floating.

The power stage circuit of the buck-boost converter is shown in Figure 3.7. The simulation result showing input voltage and current is shown in Figure 3.8.

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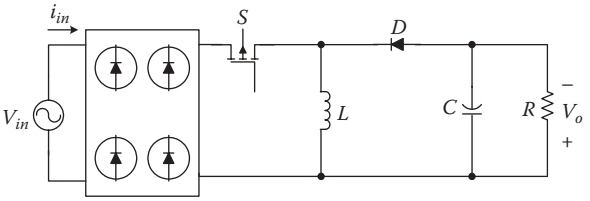


Figure 3.7 PFC buck-boost converter.

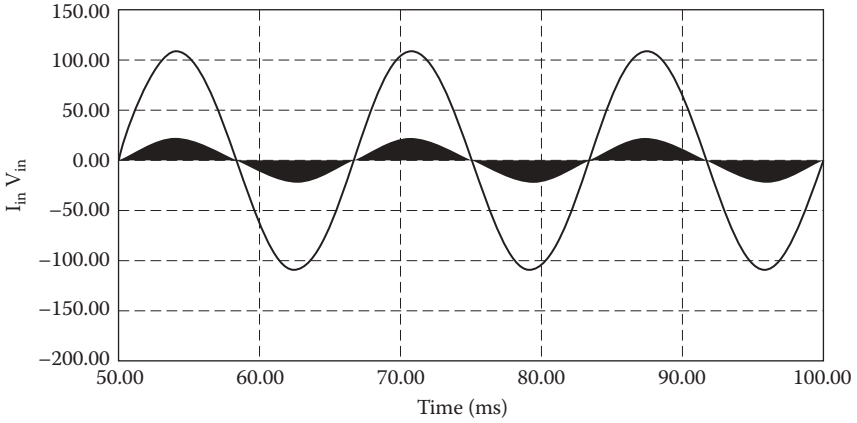


Figure 3.8 Input voltage and current for buck-boost converter as PFC.

3.3.4 Ćuk Converter as PFC

This topology is the dual of the buck-boost converter. Here also we have two inductors, one at input and the other at output. When this topology is operated in DCM-CCM (input inductor in DCM and output inductor in CCM) [7], the input current is not allowed to follow the input voltage only, and is also affected by the output current (Table 3.8). It also depends on the discharge time of the input inductor. But if it is operated in DCM-DCM mode, it is possible to achieve good power factor. Here the advantage is that the output voltage can vary independently in a specified limit as in the buck-boost topology (Figures 3.9 and 3.10).

3.3.5 SEPIC Converter as PFC

The basic structure of the SEPIC is shown in Figure 3.11. As mentioned earlier, to achieve natural power factor correction [8], it is desirable to operate the input inductor in DCM (Figure 3.12). The same applies to SEPIC. Here

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Table 3.8 Ćuk Converter

Parameter	Value
Input voltage, V_{in}	110
Switching frequency, f_s	50 k
Output voltage, V_{out}	30
Inductance, L_1	750 u
Inductance, L_2	15 u
Capacitance, C_1	5 u
Capacitance, C_2	470 u

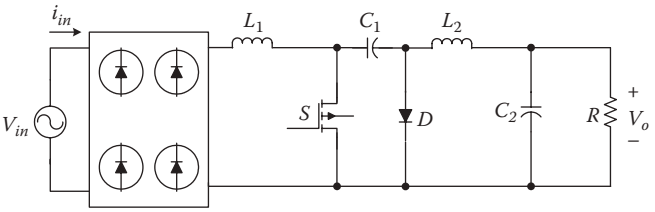


Figure 3.9 PFC Ćuk converter.

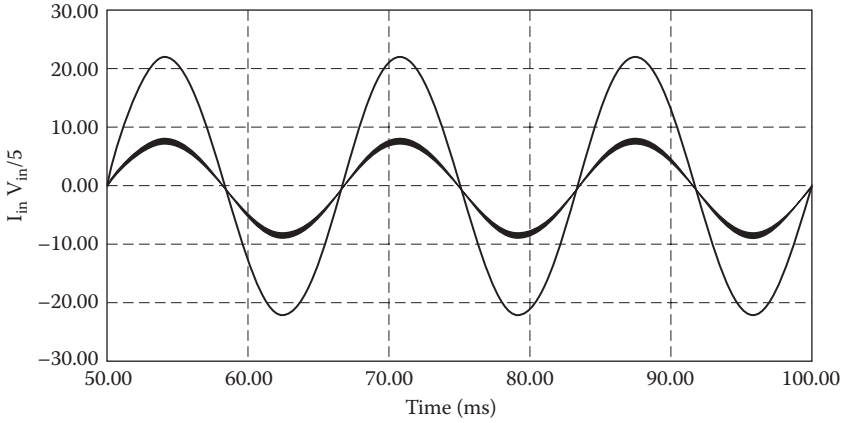


Figure 3.10 Input voltage and current of Ćuk converter as PFC.

the definition of DCM is worth noting: both the input and output inductor currents remain constant in this mode. In other words, neither of them changes its state of energy. From the state equations for this converter, it can be said that the voltage-current relationship depends on the switching frequency and duty ratio (Table 3.9). If the duty ratio and switching

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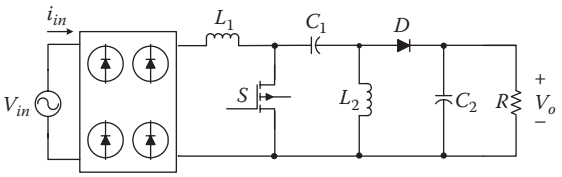


Figure 3.11 PFC SEPIC converter.

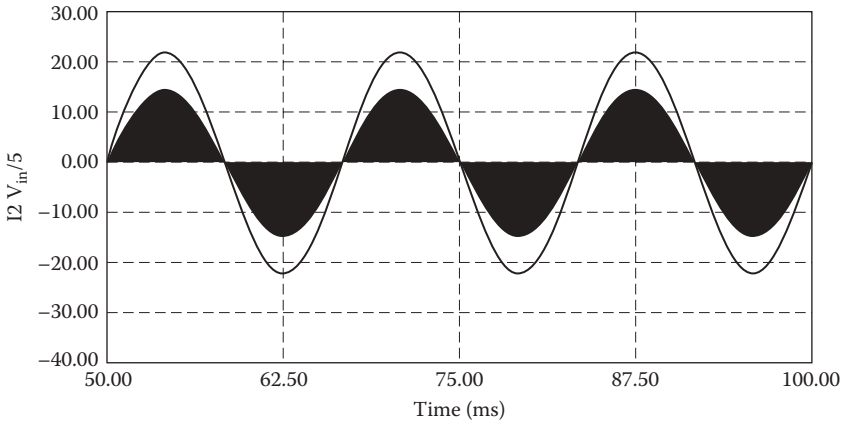


Figure 3.12 Input voltage and current of SEPIC converter as PFC.

Table 3.9 Parameters of PFC SEPIC Converter

Parameter	Value
Input Voltage, V_{in}	110
Switching frequency, f_s	50 k
Output voltage, V_{out}	50
Inductance, L_1	75 u
Inductance, L_2	150 u
Capacitance, C_1	5 u
Capacitance, C_2	500 u

frequency are kept constant, current can be forced to follow the voltage and a very high power factor can be achieved using SEPIC.

3.3.6 *Zeta Converter as PFC*

Here also the relationship between input and output voltage is similar as with buck-boost and Ćuk, although the input current is the summation of input inductor current and the output current [9], which limits its

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application to PFC (Table 3.10). This means that the state of energy of each energy storage element is not independent. The input inductor inherently makes this topology suitable when isolation is necessary, because this inductor can be utilized as a magnetizing inductance of the transformer. It also provides the feature of completely demagnetizing the transformer core. This topology is better suited for higher power applications, such as 150 to 400 W applications, than the flyback converter for the same applications.

The voltage conversion ratio or gain equation for the zeta is the same as that of the Ćuk converter and buck-boost converter. From the topology shown in Figure 3.13, it seems that the zeta converter is the dual of the SEPIC. Thus, it must give the same performance as the SEPIC converter. The simulation result for the zeta converter is shown in Figure 3.14.

3.3.7 *Flyback Converter as PFC*

With this topology the output voltage can be greater or less than the peak input voltage (Table 3.11). This can be achieved by duty ratio as well as transformer turns ratio [10]. Having the switch in series with the input provides the feature of overload protection. At the same time, it also chops the input current and generates EMI, which is to be filtered explicitly. In this topology the inductor is placed at such a location that

Table 3.10 Parameters of PFC Zeta Converter

Parameter	Value
Input voltage, V_{in}	110
Switching frequency, f_s	50 k
Output voltage, V_{out}	30
Inductance, L_1	100 u
Inductance, L_2	150 u
Capacitance, C_1	450 n
Capacitance, C_2	500 u

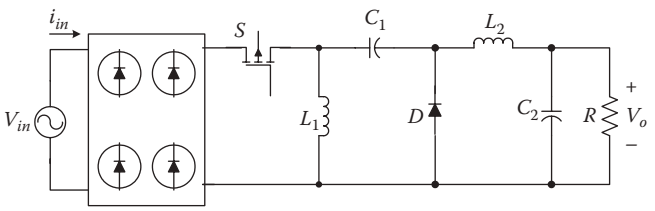


Figure 3.13 PFC ZETA converter.

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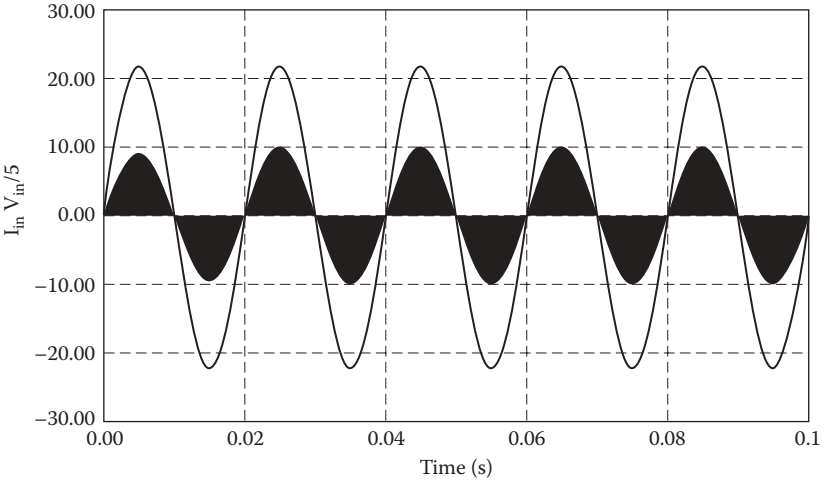


Figure 3.14 Input voltage and current of ZETA converter as PFC.

Table 3.11 Parameters of PFC Flyback Converter

Parameter	Value
Input voltage, V_{in}	110
Switching frequency, f_s	50 k
Output voltage, V_{out}	50
Inductance, L_m	20 u
Capacitance, C	600 u
Turns ratio, n	1

it can be incorporated into the power transformer to provide isolation between input and output, and have only one power magnetic component. The problem with flyback is the difficulty in programming the input current half sine wave when using current mode control (CMC). This is because CMC controls the peak inductor current, which is the input current in the boost but is not in the flyback. The input and inductor currents vary quite a bit with input voltage in the flyback topology. The solution to this problem lies in average current mode control, but the control circuit is more complex. The advantages can be summarized as follows: output can vary independently, it provides current protection, and it can provide input and output isolation. Problems can be summarized as follows: it requires a large filter for EMI, and the switch voltage rating is the sum of peak input voltage and output voltage (Figures 3.15 and 3.16).

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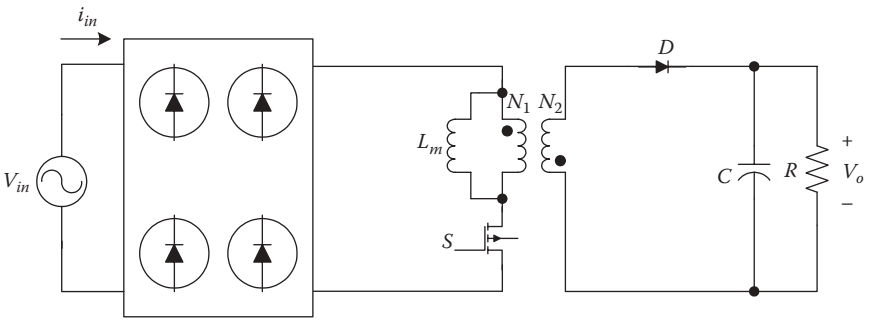


Figure 3.15 PFC flyback converter.

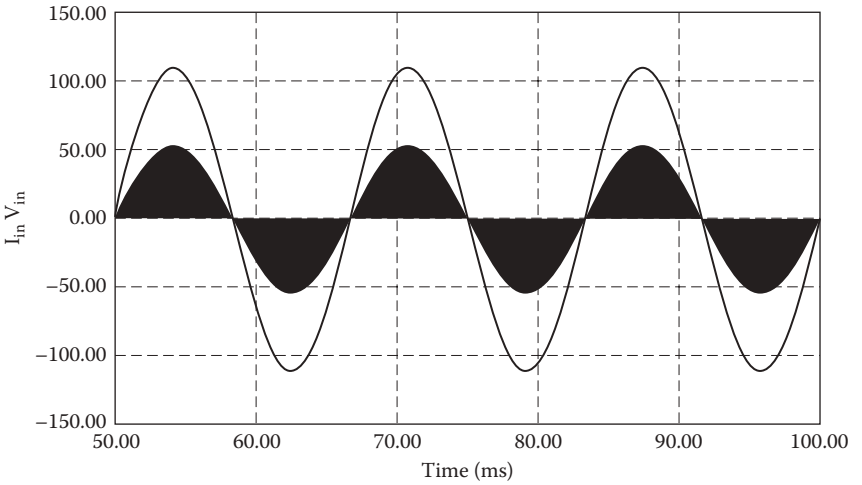


Figure 3.16 Input voltage and current of flyback converter as PFC.

3.3.8 Forward Converter as PFC

In this topology, similar to flyback topology, it is possible to achieve isolation between input and output (Table 3.12). But it is absolutely necessary to have third winding to discharge magnetizing current. Even though third winding is provided, the diode rectifier at the input prevents the negative current and one can easily conclude that this topology is not suitable for PFC in any case. This topology is much better suited for high power post regulators (Figures 3.17 and 3.18).

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Table 3.12 Forward Converter

Parameter	Value
Input voltage, V_{in}	110
Switching frequency, f_s	20 k
Output voltage, V_{out}	30
Inductance, L_o	50 u
Capacitance, C	500 u
Turns ratio, n	1

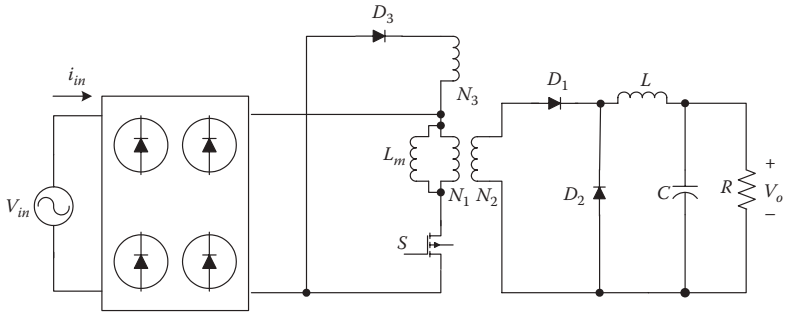


Figure 3.17 PFC forward converter.

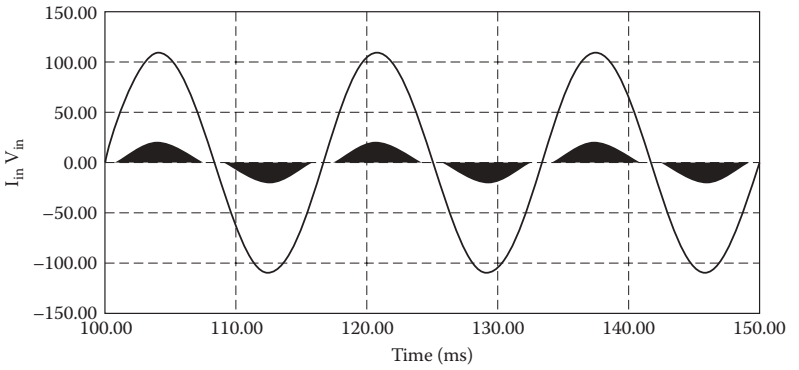


Figure 3.18 Input current and voltage of forward converter as PFC.

3.4 *Application of PFC in Advanced Motor Drives*

The switched reluctance machine (SRM) is an advanced adjustable speed device that cannot be operated by directly connecting to the mains. A power electronic interface is absolutely necessary for running it optimally. Various

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power electronic topologies have been proposed. C-dump converter topology is one of the popular topologies to drive a switched reluctance motor. As this topology contains the maximum number of passive elements and complexity, it is chosen to verify the PFC function for advanced drives, as a worst-case scenario. Figure 3.19 shows the SRM model and its driver.

In Figure 3.19, the DC source is shown as a supply for the converter and thus for the machine, although this is not the case in real life where the AC supply is available from the utility, and using either an uncontrolled or controlled rectifier, this AC is converted into DC. As mentioned in Section 3.3, when only Diode Bridge Rectifier (DBR) is connected between the drive and utility, the smoothing capacitor gets charged and discharged during the high line periods, and during that short time, high current spikes occur and the same spikes appear across the utility side. This will deteriorate both power factor and overall system performance. Figures 3.20 and 3.21 explain the power stages of such an uncontrolled DC link and its operating waveforms. From the supply voltage and current waveforms shown, it is clear that extensive distortion occurs on the supply side.

As mentioned in the previous sections, the boost converter is the best-suited topology for active power factor correction. Figure 3.22 shows the power stage diagram and simulation result of an SRM drive with a boost converter as PFC.

From the waveforms shown in Figure 3.23 and by using a DC-DC boost converter, almost unity power factor can be achieved and the load to the converter appears almost resistive, no matter how many passive

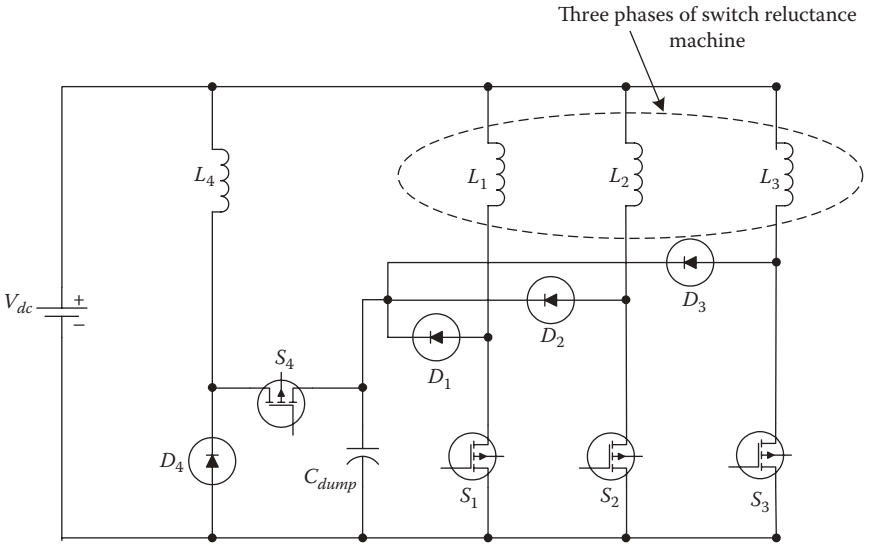


Figure 3.19 C-dump converter as SRM driver.

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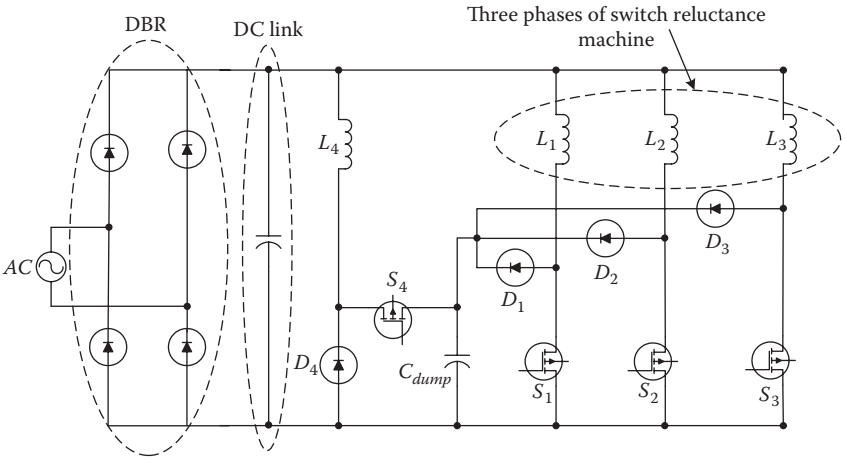


Figure 3.20 SRM drive with simple diode bridge rectifier as DC link.

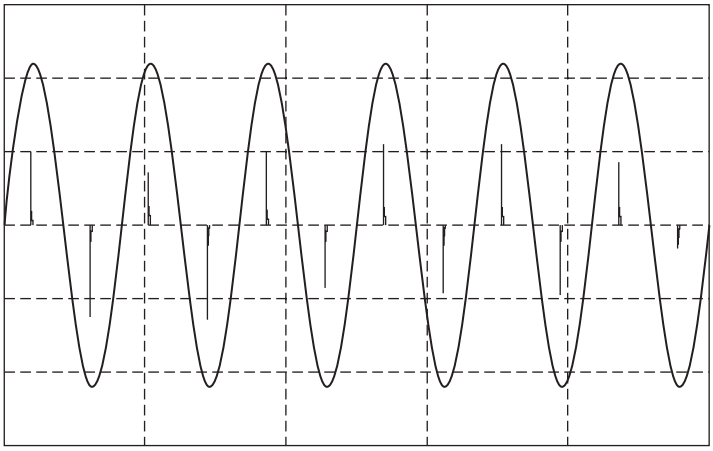


Figure 3.21 Input voltage and current of SRM when DBR is used as DC link.

components it contains. No current peaks are visible in the supply current waveform. Explanation of the detailed operation of the boost converter can be found in the references.

Here, the boost converter switch is controlled, keeping output voltage of the converter in mind, and it has nothing to do with controlling the switches of the main SRM drive circuit. But during dynamic conditions it should be observed that the overall system is not going to be unstable. Sometimes all the switches in a system are synchronized to avoid this problem. By modulating the duty cycle of the boost converter switch, the

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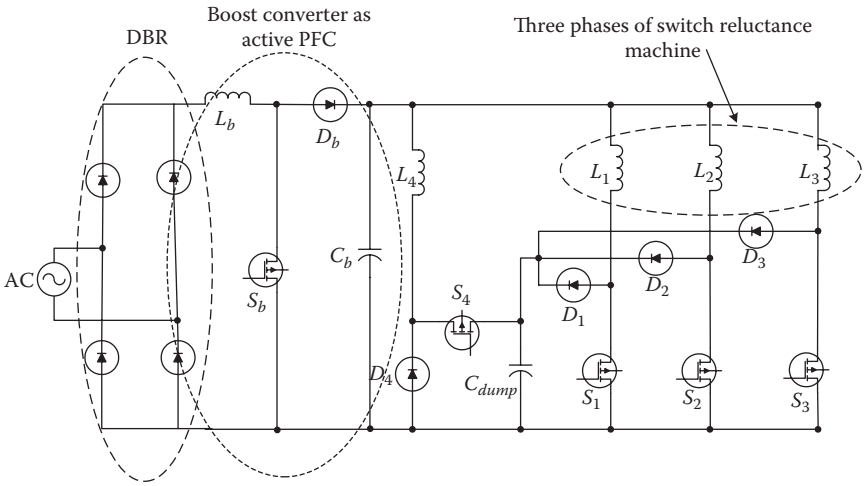


Figure 3.22 SRM drive with boost converter for PFC at front end.

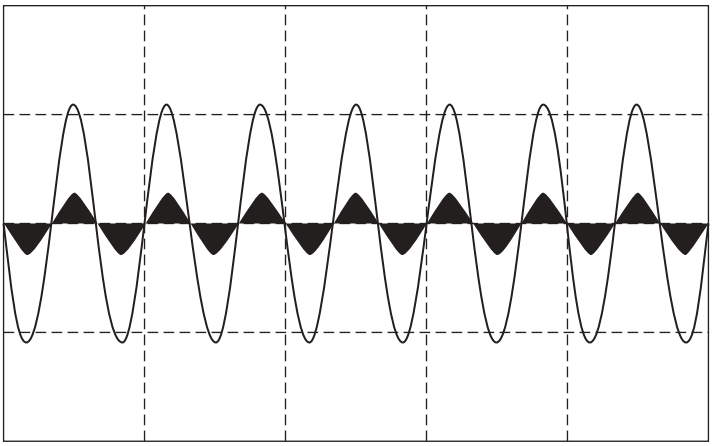


Figure 3.23 V_{in} and I_{in} of SRM with boost converter as PFC at front end.

input current can be controlled to track the input voltage. With low distortion and accurate tracking between current and voltage, the power factor obtained from adding a front-end boost converter is typically higher than 99% and the input current THD is normally less than 5%.

In this chapter, the reasons for employing power factor correction techniques and various methods of PFCs and their effectiveness are discussed. Simulation results have been provided to justify the theoretical analysis. International and IEEE standards impose limits on harmonic voltage and current. Many power electronics circuit designs have been proposed to

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deal with these standards. Compliance with the IEC standards has been studied with computer simulations. The effectiveness of active PFC is normally not a problem, but the cost involved in the additional power electronics circuit could be a major obstacle to acceptance. The simplest power factor correction method is to use a passive method, for example, an L-C filter, to comply with IEC and IEEE standards. Although using these passive PFC methods complies with standards found satisfactory, the problems of EMI, electromagnetic compatibility (EMC), and the size of the passive elements involved in them are to be justified. Thus, the final sentence of this chapter will be, "How to design a cost-effective power electronics equipment that will comply with harmonic standards and not introduce side effects or system interaction problems remains an open challenge to power electronics engineers."

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chapter four

Integrated Switched-Mode Power Converters

4.1 Switched-Mode Power Supplies

Switched-mode power supplies (SMPs) have been used for many years in industrial and aerospace applications where good efficiency, light weight, and small size are of prime concern.

An SMPS offers three main advantages over a conventional linear power supply: high efficiency and less heat generation, tighter regulation, and small size and weight. Conventional linear power suppliers are inefficient because they regulate by dumping the excess power into heat. Conventional linear power supplies are typically 40%–50% efficient, while switches have efficiencies from 60%–90%. Another key benefit of SMPSs is their ability to closely regulate the output voltage. Switched-mode supplies regulate continuously and follow load changes almost immediately. In addition, switchers have the unique ability to maintain the correct output under low input conditions. In fact, switchers can actually produce an output voltage that is higher than the DC voltage applied to the input. A final advantage of switchers is their relatively small size and weight. Because switches operate at high frequencies, the parts are smaller than those needed for a conventional 60 Hz power supply of small power rating. The transformers, capacitors, and coils are also physically smaller and lighter [1]-[5].

There are many important applications for switched mode power supplies. They are widely used in the following fields [5]-[15]:

- DC-DC converter + motor drives
- Active filter + UPS
- PFC + DC-DC converter
- Inductor heater
- Ballast application

The system construction of traditional switched mode power supplies in a PFC + DC-DC converter is shown in Figure 4.1.

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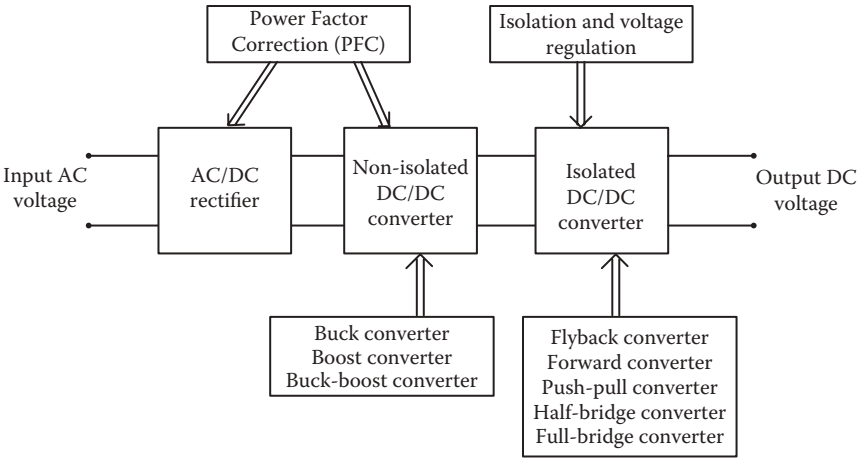


Figure 4.1 System construction for conventional SMPS.

There are two kinds of general control methods for switched mode DC-DC power supplies. One is voltage mode control. The other one is the current mode control. There are three current control methods: tolerance band control, constant off time control, and constant frequency with turn on at clock time [16]–[19]. They are shown in Figures 4.2 through 4.6.

4.2 Concept of Integrated Converter

To build the conventional switched mode power supply, practice is to cascade the separate power electronics converters, then debug and test the circuit stage by stage. Compared to the line power supply, this method does have advantages for using the high switching frequency [10], [11].

With the demand for higher efficiency, smaller output ripple, and smaller converter size, as well as some other new requirements for modern

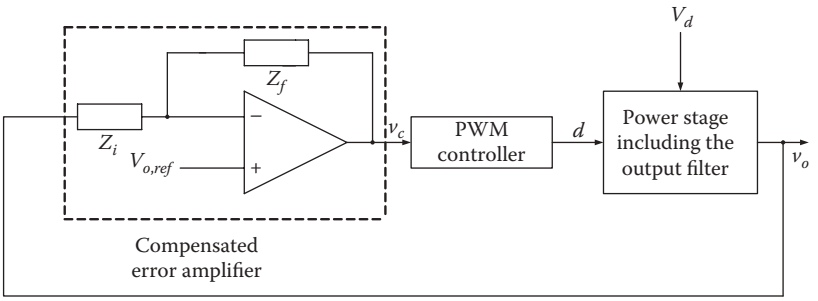


Figure 4.2 Control construction for SMPS.

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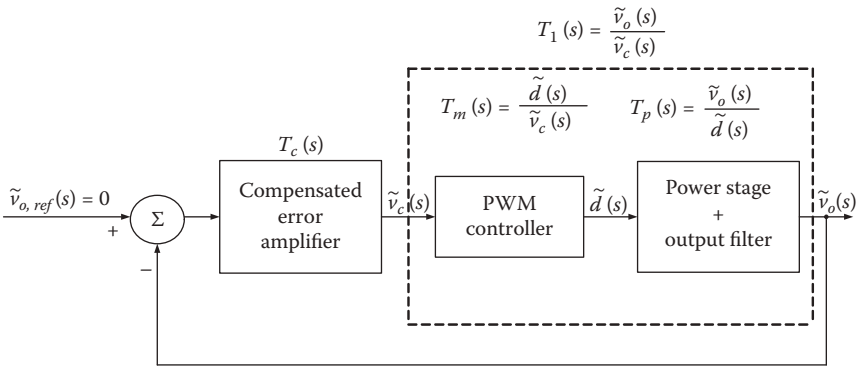


Figure 4.3 Transfer function-based control method for SMPS.

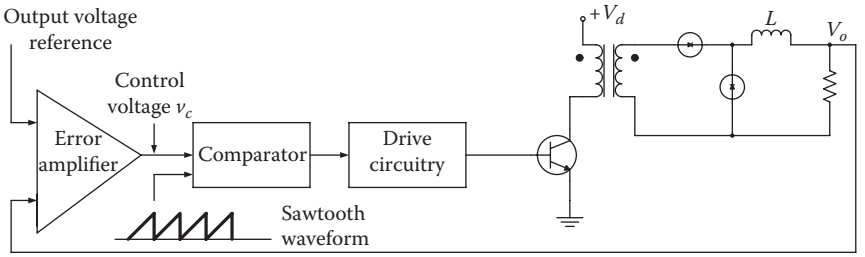


Figure 4.4 Voltage mode control for SMPS.

power electronics systems, the conventional switched-mode power supply can be further improved by employing an integrated converter.

An integrated converter is a synthesized device based on the overall system integration, which is simplified by the system objective and can implement the system functions similar to the discrete converters without integration.

Simplification means the process of synthesizing converters with reduced components, smaller size, and lower weight or cost. System objectives can include minimum cost, maximum efficiency, high reliability, low switch stress and power packing, wide conversion range, PFC and output regulation, inverter PFC, and better performance.

4.2.1 *Integrated Converter Configuration*

Figure 4.7 shows a simplified model for an integrated converter. A detailed model for an integrated converter is presented in Figure 4.8 and shows the difference between basic converters and integrated converters. Integrated converters consist of converter sets, and each converter set has a special

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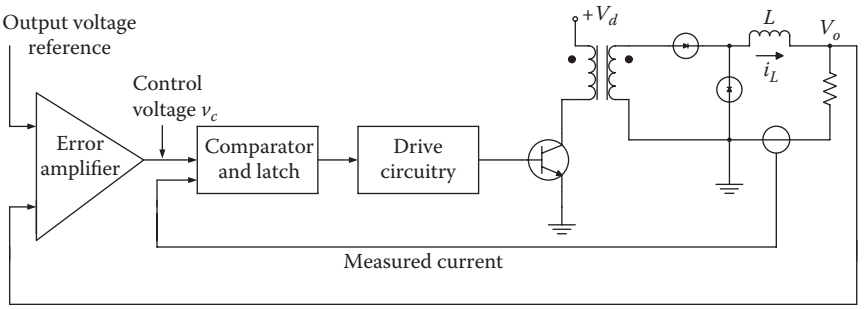


Figure 4.5 Current mode control for SMPS.

function required by users. Integrated converters own at least two converter sets, and the basic converters, such as buck and boost, only own one converter set. In general, every converter set has some relationship with the other. However, in most situations in power electronics applications, the general model shown in Figure 4.9 for the integrated converter is used.

It can be seen from the configuration of integrated converters that the integrated converter not only owns all discrete functions of every converter set, but also has a simplification process based on the system integration. Care should be taken that each discrete converter set can be a sub-integrated converter or basic converter. This kind of sub-integrated converter is based on the integration of every sub-building block. The integrated converter is based on the integration of a sub-integrated converter [5]. It means that the integrated converter is based on the system integration.

4.3 *Definition of Integrated Switched-Mode Power Supplies (ISMPS)*

Integrated switched-mode power supply (ISMPS) is based on the integrated converter concept. The application field for conventional switched-mode power supplies is also suitable for integrated switched-mode power supplies. The traditional cascade power converter is replaced by an integrated power converter. In this way, the new power supplies can have higher efficiency or higher density or smaller size or better output regulation than traditional switched-mode power supplies [10], [11].

Integrated converters can not only implement the system functions similar to the discrete converters without integration, but they also have other special functions. For example, BIFRED converters [20]–[22], on one hand, can have the functions of boost cascaded flyback converters. On the

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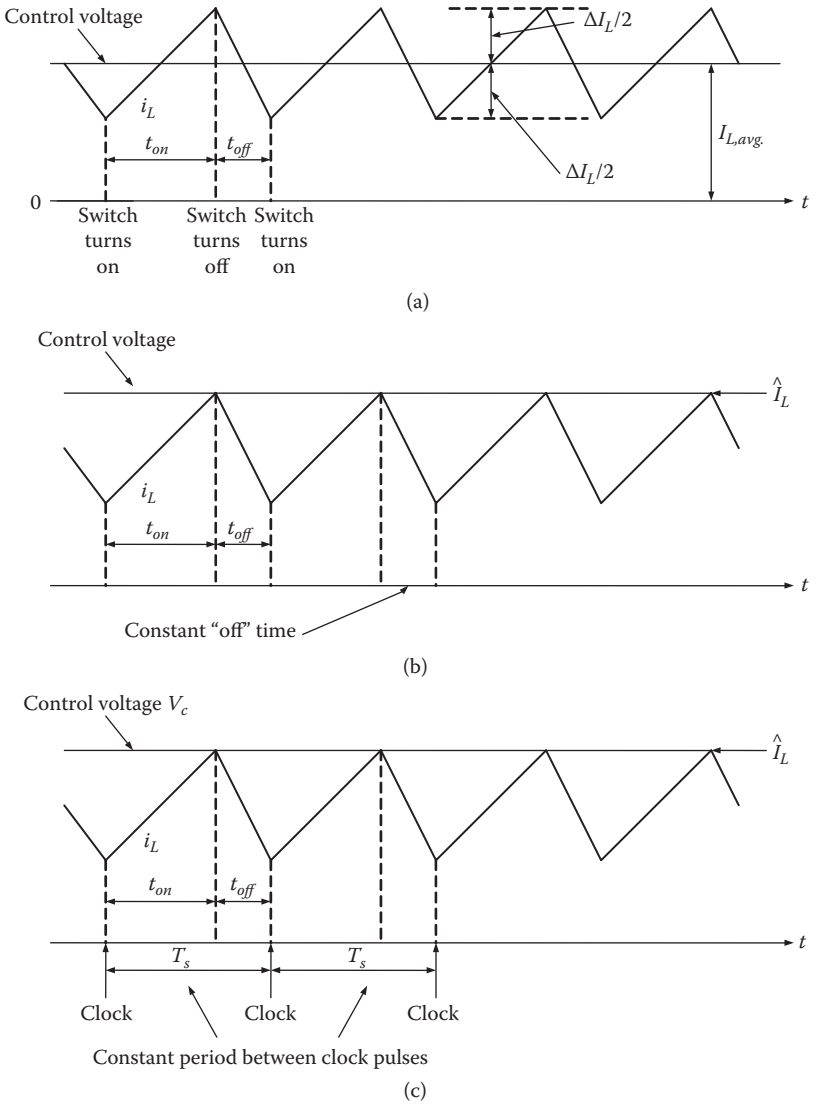


Figure 4.6 Different current mode control methods (a) tolerance band control (b) constant off time, and (c) constant frequency at turn-on at clock time

other hand, they can have wider range for output voltage regulation and higher power density.

Integrated converters can be classified into four types. There are boost type integrated topologies, buck type integrated topologies, buck-boost

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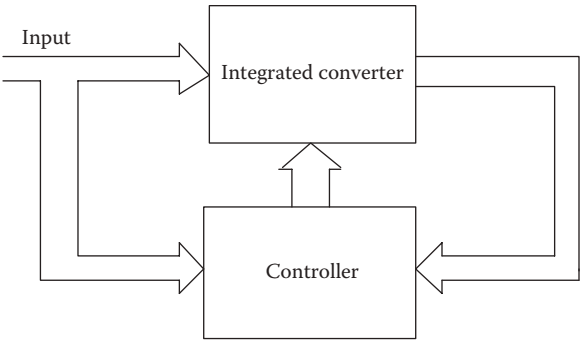


Figure 4.7 Simplified model for integrated converter.

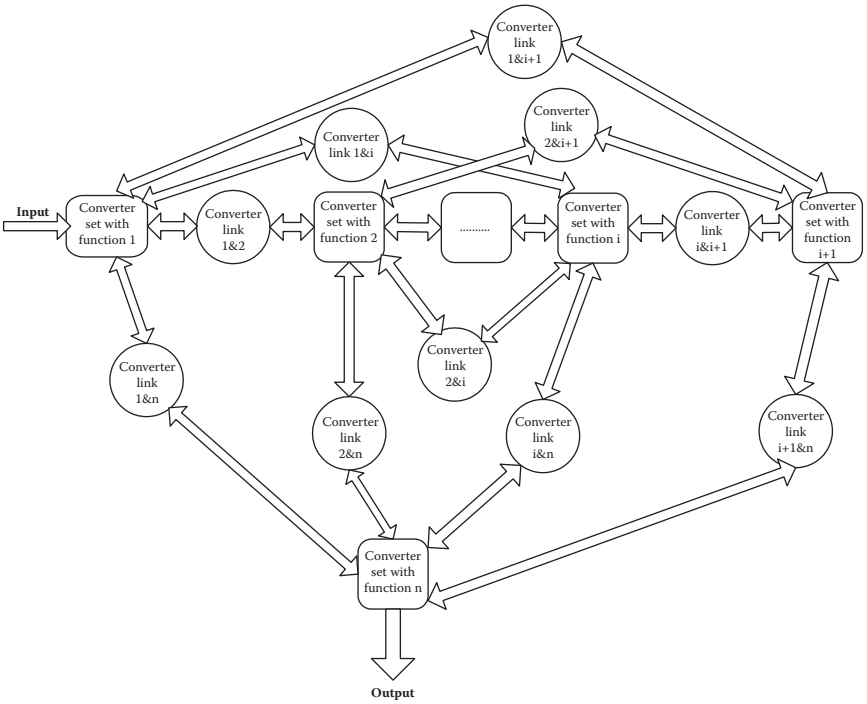


Figure 4.8 Detailed model for integrated converter.

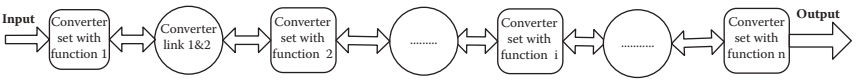


Figure 4.9 General model for integrated converter.

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type integrated topologies, and other type. Each of them will be introduced in the following chapters.

The control methods for the conventional switched-mode power supplies are also suitable for the integrated converters, which have more complicated transfer functions. New, flexible control methods are also needed.

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chapter five

Boost-Type Integrated Topologies

5.1 General Structure of Boost-Type Integrated Topologies

For this type of integrated system, the boost converter is in the front and is followed by another basic non-isolated or isolated converter. Both of them share one active switch. The output of the boost converter will be used as the input source for the second converter. When the switch is on, the boost inductor is charged. The second converter will also work in the switch-on state. When the switch is off, the inductor is discharged. The sum of the input source energy and the inductor storage energy will be transferred to the boost output [1]–[7].

Based on the different operation modes for the inductors in the converter, the circuit will work in the mode of CCM-CCM, CCM-DCM, DCM-CCM, and DCM-DCM.

5.2 Boost-Flyback Converter

The boost-flyback converter is shown in Figure 5.1. The boost converter consists of inductance L_{in}, diode D_1, diode D_2, switch Q, capacitor C_1, and input source v_s.

The flyback converter consists of the capacitor C_1, switch Q, transformer, diode D_3, output capacitor C_{out}, and load resistor R where the flyback converter and boost converter share a common switch Q. The input source V_{c1} for the flyback converter is from the output of the boost converter.

5.3 Boost–Double-Ended Flyback Converter

This topology is presented in Figure 5.2. The boost converter consists of inductance L_{in}, diode D_1, diode D_2, switch Q_2, capacitor C_1, and input source v_s. The double-ended flyback converter consists of the capacitor C_1, switch Q_1, switch Q_2, transformer, diode D_3, output capacitor C_{out}, and load resistor R where double-ended flyback converter and boost converter share a common switch Q_2. The input source V_{c1} for the double-ended flyback converter is from the output of the boost converter.

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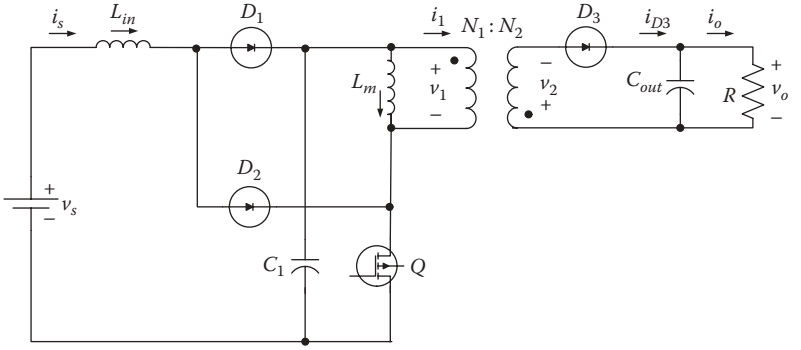


Figure 5.1 Boost-flyback converter.

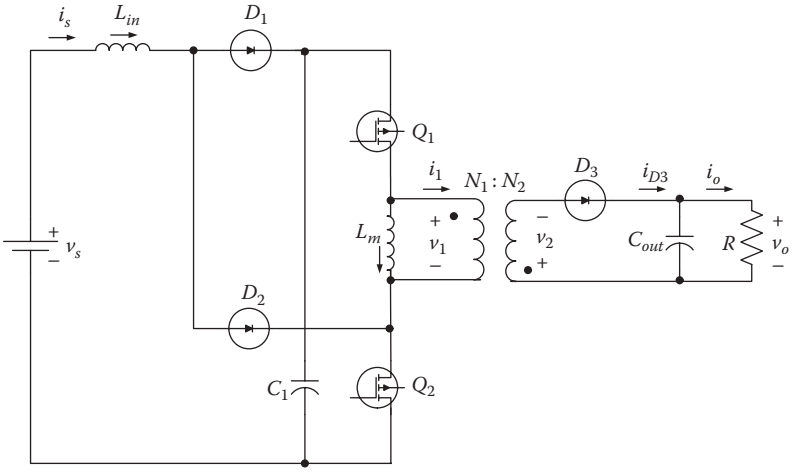


Figure 5.2 Boost double-ended flyback converter.

5.4 *Boost Series Parallel Flyback Converter*

As shown in Figure 5.3, the boost converter consists of inductance L_{in}, diode D_2, switch Q_1, capacitor C_1, capacitor C_2, and input source v_s.

The series/parallel flyback converter consists of the capacitor C_1, capacitor C_2, switch Q_1, transformer, diode D_1, diode D_2, diode D_3, diode D_4, output capacitor C_{out}, and load resistor R where the series/parallel flyback converter and boost converter share a common switch Q_1. The input source V_{c1} and V_{c2} for the series/parallel flyback converter is from the output of the boost converter.

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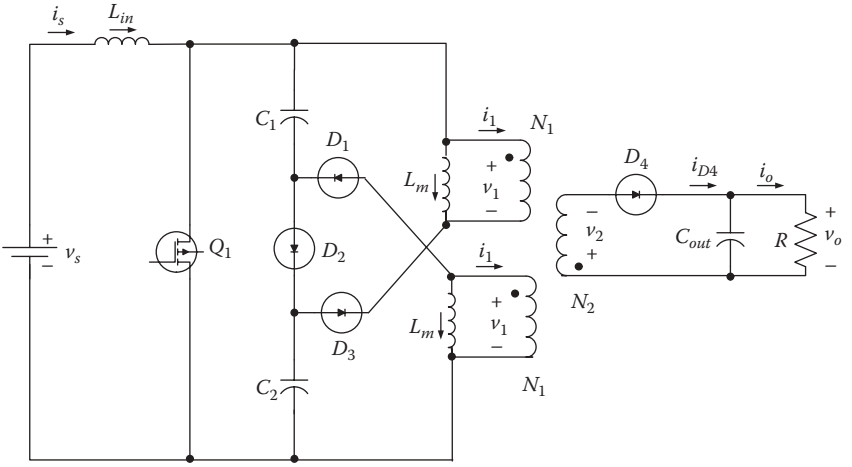


Figure 5.3 Boost series parallel flyback converter.

5.5 *Boost–Parallel Flyback Converter*

Presented in Figure 5.4, the boost converter consists of inductance L_{in}, diode D_1, diode D_2, switch Q_1, capacitor C_1, and input source v_s.

The parallel flyback converter consists of the capacitor C_1, switch Q_1, switch Q_2, transformers, diode D_3, diode D_4, output capacitor C_{out}, and load resistor R where the parallel flyback converter and boost converter share a common switch Q_1. The input source V_{c1} for the parallel flyback converter is from the output of the boost converter.

5.6 *Boost–Forward Converter*

The boost converter consists of inductance L_{in}, diode D_1, diode D_2, switch Q, capacitor C_1, and input source v_s, as shown in Figure 5.5.

The forward converter consists of capacitor C_1, switch Q, transformer, diode D_3, diode D_4, output inductance L_{out}, output capacitor C_{out}, and load resistor R where the forward converter and boost converter share a common switch Q. The input source V_{c1} for the forward converter is from the output of the boost converter.

5.7 *Boost–Double-Ended Forward Converter*

The boost converter consists of inductance L_{in}, diode D_1, diode D_2, switch Q_2, capacitor C_1, and input source v_s.

The double-ended forward converter consists of the capacitor C_1, switch Q_1, switch Q_2, transformer, diode D_3, diode D_4, output inductance

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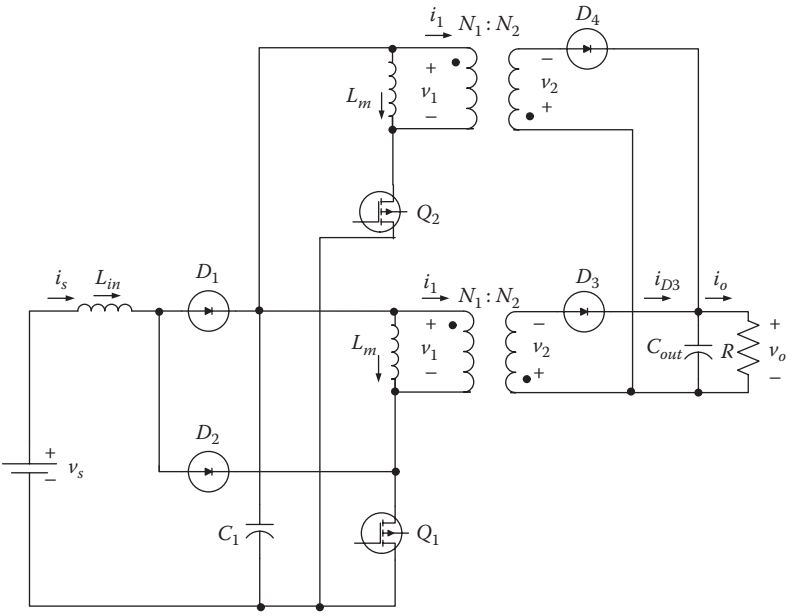


Figure 5.4 Boost-parallel flyback converter.

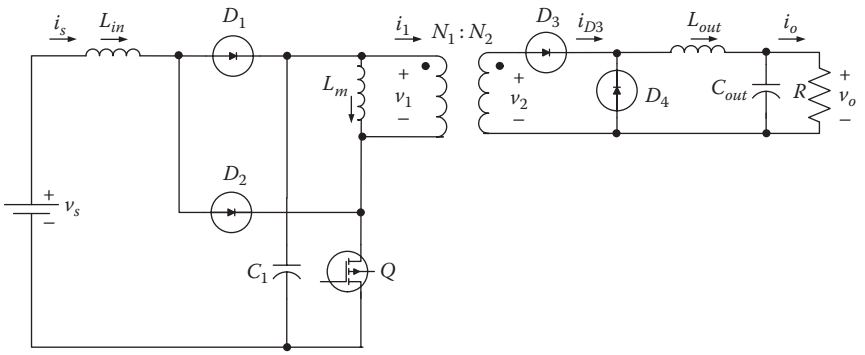


Figure 5.5 Boost-forward flyback converter.

L_{out}, output capacitor C_{out}, and load resistor R, where the double-ended forward converter and boost converter share a common switch Q_2. The input source V_{c1} for the double-ended forward converter is from the output of the boost converter. This converter is shown in Figure 5.6.

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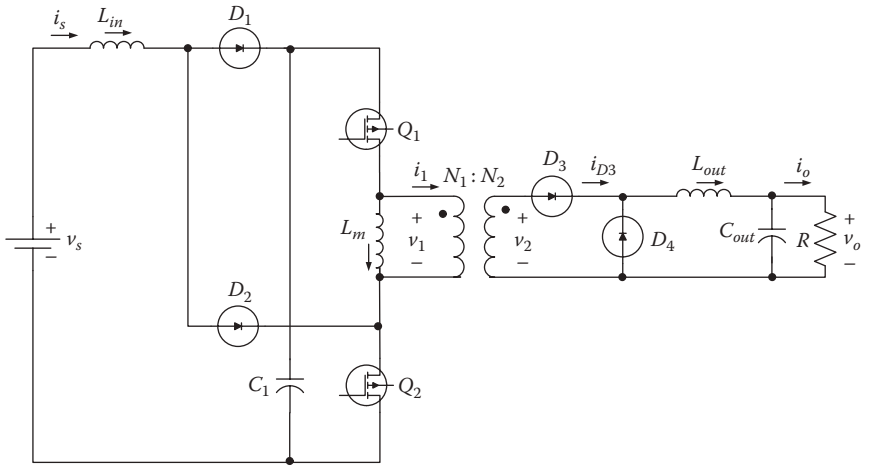


Figure 5.6 Boost double-ended forward converter.

5.8 *Boost Series Parallel Forward Converter*

The topology of the boost series parallel forward converter is presented in Figure 5.7. The boost converter consists of inductance L_{in}, diode D_2, switch Q_1, capacitor C_1, capacitor C_2, and input source v_s.

The series parallel forward converter consists of the capacitor C_1, capacitor C_2, switch Q_1, transformer, diode D_1, diode D_2, diode D_3, diode D_4, output inductance L_{out}, output capacitor C_{out}, and load resistor R where the series parallel forward converter and boost converter share a common

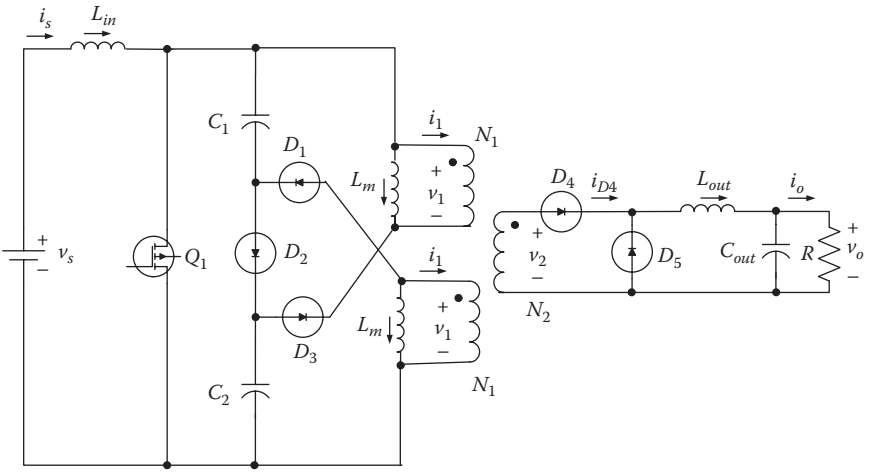


Figure 5.7 Boost series parallel forward converter.

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switch Q_1. The input source V_{c1} and V_{c2} for the series parallel forward converter is from the output of the boost converter.

5.9 Boost–Parallel Forward Converter

As illustrated in Figure 5.8, the boost converter consists of inductance L_{in}, diode D_1, diode D_2, switch Q_1, capacitor C_1, and input source v_s.

The parallel forward converter consists of the capacitor C_1, switch Q_1, switch Q_2, transformers, diode D_3, diode D_4, diode D_5, diode D_6, output inductance L_{out}, output capacitor C_{out}, and load resistor R, where the parallel forward converter and boost converter share a common switch Q_1. The input source V_{c1} for the parallel forward converter is from the output of the boost converter.

5.10 Boost–Full-Bridge Converter

As shown in Figure 5.9, the boost converter consists of inductance L_{in}, diode D_1, diode D_2, switch Q_2, capacitor C_1, and input source v_s.

The full-bridge converter consists of the capacitor C_1, switch Q_1, switch Q_2, switch Q_3, switch Q_4, transformer, diode D_3, diode D_4, output inductance L_{out}, output capacitor C_{out}, and load resistor R, where

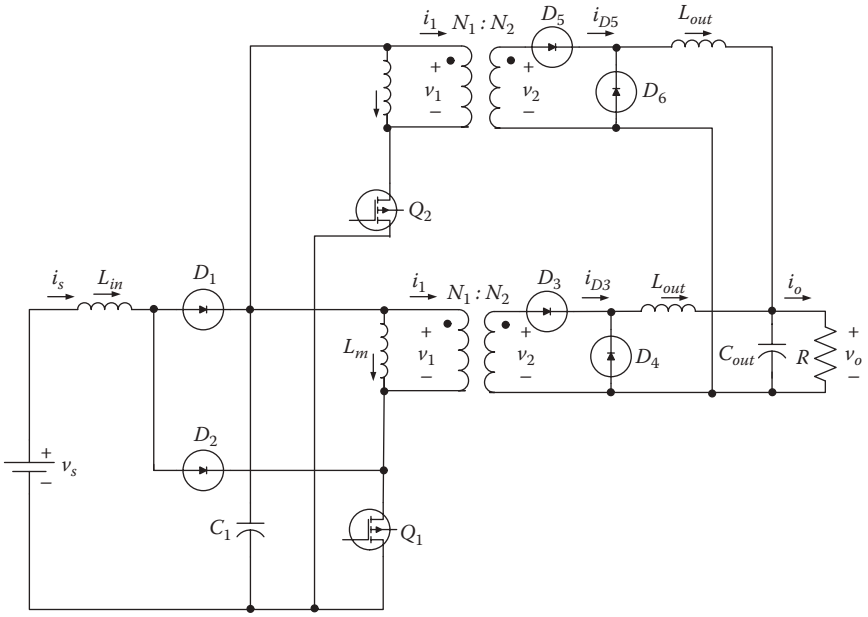


Figure 5.8 Boost parallel forward converter.

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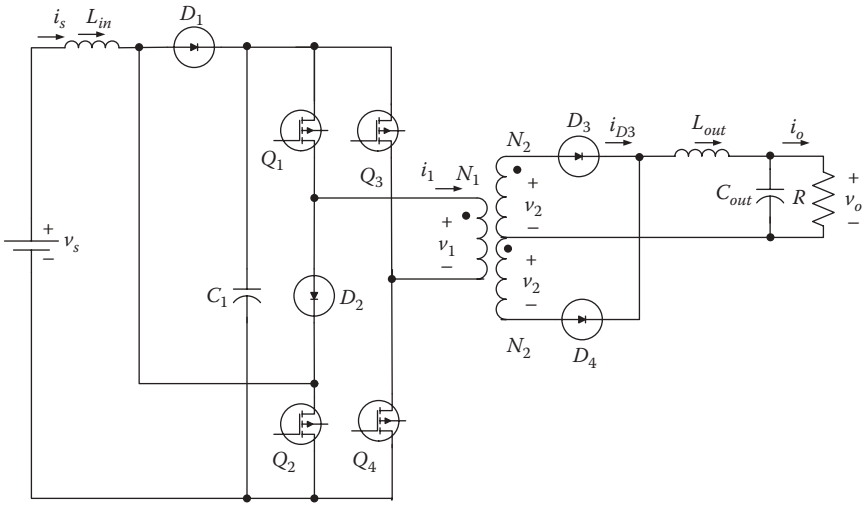


Figure 5.9 Boost–full bridge converter.

the full-bridge converter and boost converter share a common switch Q_2. The input source for the full-bridge V_{c1} is from the output of the boost converter.

5.11 Boost–Half-Bridge Converter

The boost converter consists of inductance L_{in}, diode D_1, switch Q_2, capacitor C_1, capacitor C_2, and input source v_s. This is shown in Figure 5.10.

The half-bridge converter consists of the capacitor C_1, capacitor C_2, switch Q_1, switch Q_2, transformer, diode D_2, diode D_3, diode D_4, output inductance L_{out}, output capacitor C_{out}, and load resistor R, where the half-bridge converter and boost converter share a common switch Q_2. The input source for the half-bridge V_c is from the output of the boost converter.

5.12 Boost–Push-Pull Converter

The boost converter consists of inductance L_{in}, diode D_1, diode D_2, switch Q_1, capacitor C_1, and input source v_s, as shown in Figure 5.11.

The push-pull converter consists of the capacitor C_1, switch Q_1, switch Q_2, transformer, diode D_3, diode D_4, output inductance L_{out}, output capacitor C_{out}, and load resistor R, where the push-pull converter and boost converter share a common switch Q_1. The input source for the push-pull V_{c1} is from the output of the boost converter [7].

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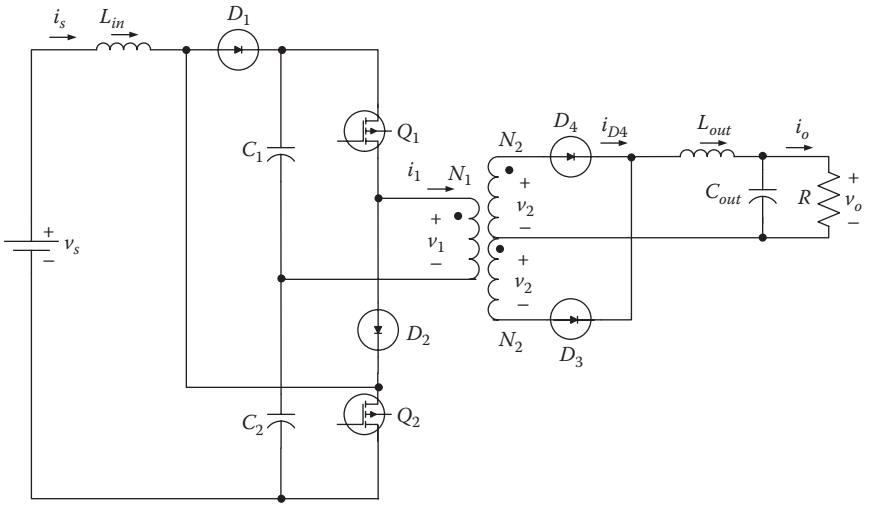


Figure 5.10 Boost–half bridge converter.

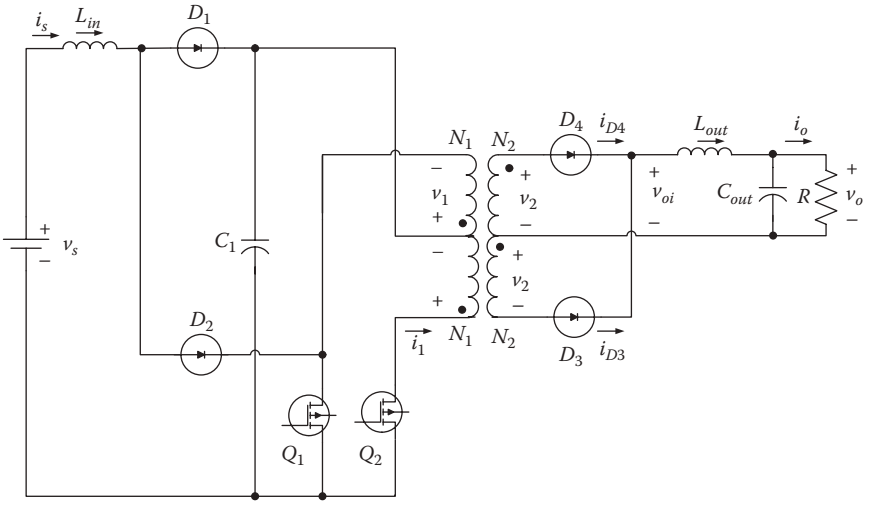


Figure 5.11 Boost–push pull converter.

5.13 *Boost–Buck-Boost Converter*

The buck-boost converter can be non-isolated or isolated. When it is non-isolated, the circuit will become a SEPIC converter, as shown in Figure 5.12.

The SEPIC converter is a single-ended primary inductance device (Figure 5.13). This converter uses two inductances. The front end acts as

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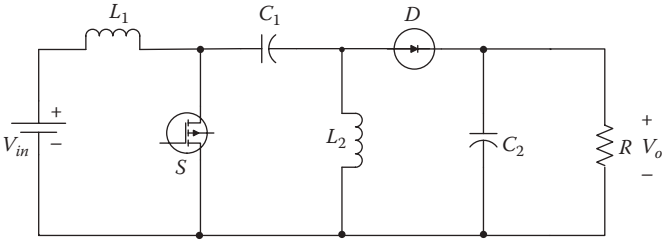


Figure 5.12 Non-isolated SEPIC converter.

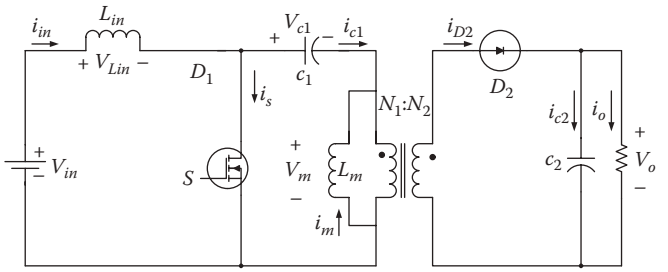


Figure 5.13 Isolated SEPIC converter.

the boost topology, while the back end has the function of a buck-boost or flyback converter. The steady state average voltage across C_1 is always equal to the input voltage V_{in}.

The SEPIC converter has a special advantage in high power factor pre-regulation applications. If two inductors are coupled, ripple current steering can be achieved.

5.14 *Boost Integrated Flyback Rectifier/ Energy Storage Converter*

The boost integrated flyback rectifier/energy storage DC-DC (BIFRED) integrates boost and flyback converter topologies, which is shown in Figure 5.14. It can be clearly observed that it closely resembles the SEPIC converter in isolated form. The only difference is the input diode in series with the input inductor. This diode prevents the negative current flow in the line. Therefore, it is possible to achieve those operating modes that are not possible with the isolated SEPIC converter [2]-[3].

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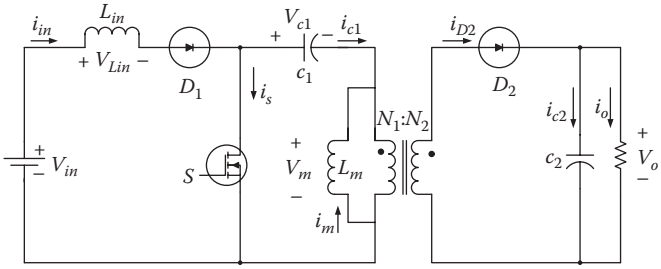


Figure 5.14 BIFRED converter.

5.15 Boost-Buck Converter (Ćuk Converter)

The front side (Figure 5.15) is a boost converter. For the buck converter, it can be non-isolated or isolated. When it is non-isolated, the circuit will become a non-isolated Ćuk converter.

With what Dr. Ćuk termed "the topological reduction of the switch," this topology features a single grounded switch, and unlike the cascade, it is easily isolated and provided with multiple outputs of either polarity. Due to the energy transfer cap's ability to store charge statically, it features capacitive energy transfer for high efficiency.

The correct use of this topology is as a regulator in a standard power supply, whether off-line or from a DC source. It is also suitable for inverting on-board regulators, complementing the boost-buck cascade.

To null output ripple, the two inductors may be coupled. Winding them on the same core with a gap to reduce the coupling coefficient to $0.9 < k < 1.0$ and reducing the primary side turns slightly produces the desired effect. The procedure yields a control function with a single RHP zero, which cannot be damped out. The lack of output ripple eliminates high frequency heating of the speaker magnet, leaving a clean output waveform.

If an isolation transformer is used in this converter, two inductors and the transformer can be integrated. This will result in zero input and output ripple. In this case, the converter is ideal for the practical model of a DC transformer.

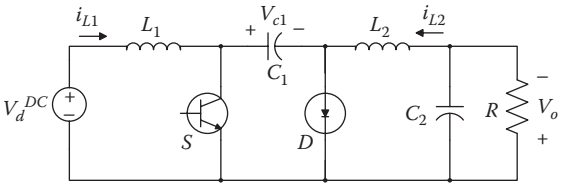


Figure 5.15 Ćuk converter.

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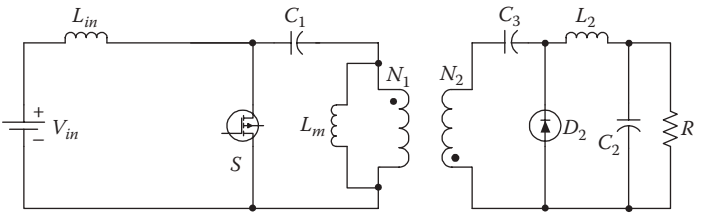


Figure 5.16 Isolated Ćuk converter.

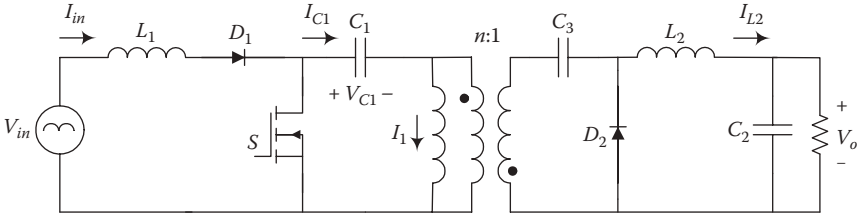


Figure 5.17 BIBRED converter.

$$V_{C1} = V_d + V_o \tag{5.1}$$

When the buck-boost converter is non-isolated, the circuit will become an isolated Ćuk converter (Figure 5.16).

5.16 *Boost Integrated Buck Rectifier/ Energy Storage Converter*

The boost integrated buck rectifier/energy storage DC-DC (BIBRED) integrates boost and buck converter topologies (Figure 5.17). It can be clearly observed that it closely resembles the Ćuk converter in isolated form. The only difference is that the input diode is in series with the input inductor [4]. This input diode prevents the negative current flow in the line. Therefore, it is possible to achieve those operating modes that are not possible with the isolated Ćuk converter.

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chapter six

Buck-Type Integrated Topologies

6.1 Concept of Boost-Integrated Converter

For this type of integrated converter, the buck converter is in the front followed by another basic non-isolated or isolated converter. Both of them share one active switch. The output of the buck converter will be used as the input source for the second converter. When the switch is on, input source energy will transfer to the buck output. The second converter will also work in the switch on state. When the switch is off, input source energy for the buck converter is disconnected from the buck output [1]-[5]. Based on the different operation modes for the inductors in the converter, the circuit will work in the mode of CCM-CCM, CCM-DCM, DCM-CCM, and DCM-DCM.

6.2 Buck Flyback Converter

The structure of the buck-flyback converter is shown in Figure 6.1. The buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q, capacitor C_1, and input source v_s.

The flyback converter consists of the capacitor C_1, switch Q, transformer, and diode D_2, diode D_3, diode D_4, output capacitor C_{out}, and load resistor R where the flyback converter and buck converter share a common switch Q. The input source V_{c1} for the flyback converter is from the output of the buck converter [1].

6.3 Buck Double-Ended Flyback Converter

As shown in Figure 6.2, in this topology the buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q_1, capacitor C_1, and input source v_s.

The double-ended flyback converter consists of the capacitor C_1, switch Q_1, and switch Q_2, transformer, diode D_2, diode D_3, diode D_4, output capacitor C_{out}, and load resistor R where the double-ended flyback converter and buck converter share a common switch Q_2. The input source V_{c1} for the double-ended flyback converter is from the output of the buck converter [1].

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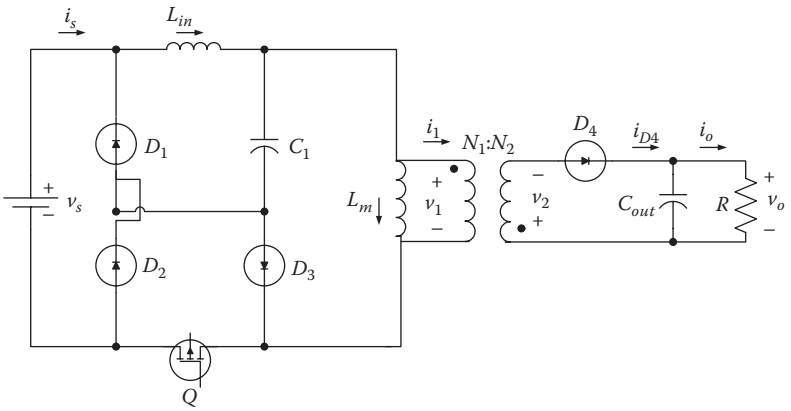


Figure 6.1 Buck flyback converter.

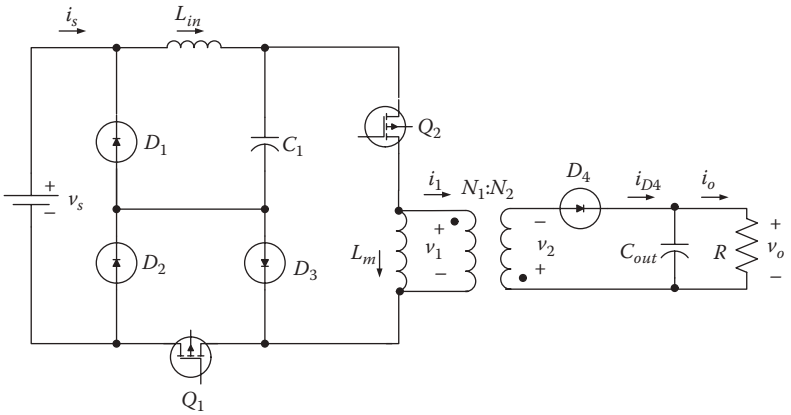


Figure 6.2 Buck double-ended flyback converter.

6.4 *Buck–Series/Parallel Flyback Converter*

Figure 6.3 shows that the buck converter consists of inductance L_{in}, diode D_1, diode D_2, diode D_3, diode D_5, switch Q_1, capacitor C_1, capacitor C_2, and input source v_s.

The series/parallel flyback converter consists of the capacitor C_1, capacitor C_2, switch Q_1, transformer, diode D_1, diode D_2, diode D_3, diode D_4, output capacitor C_{out}, and load resistor R, where the series/parallel flyback converter and buck converter share a common switch Q_1. The input

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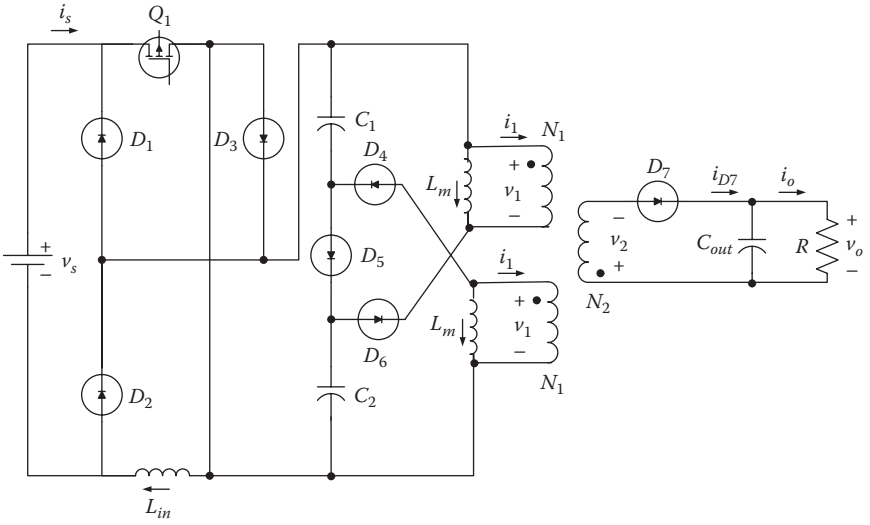


Figure 6.3 Buck series parallel flyback converter.

source V_{c1} and V_{c2} for the series/parallel flyback converter is from the output of the buck converter [1].

6.5 Buck Parallel Flyback Converter

In this configuration, shown in Figure 6.4, the buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q_1, capacitor C_1, and input source v_s.

The parallel flyback converter consists of the capacitor C_1, switch Q_1, switch Q_2 transformers, diode D_2, diode D_3, diode D_4, diode D_5, output capacitor C_{out}, and load resistor R, where the parallel flyback converter and buck converter share a common switch Q_1. The input source V_{c1} for the parallel flyback converter is from the output of the buck converter.

6.6 Buck Forward Converter

As shown in Figure 6.5, the buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q, capacitor C_1, and input source v_s.

The forward converter consists of capacitor C_1, switch Q, transformer, diode D_3, diode D_4, diode D_5, output capacitor C_{out}, output inductor L_{out}, and load resistor R, where the forward converter and boost converter

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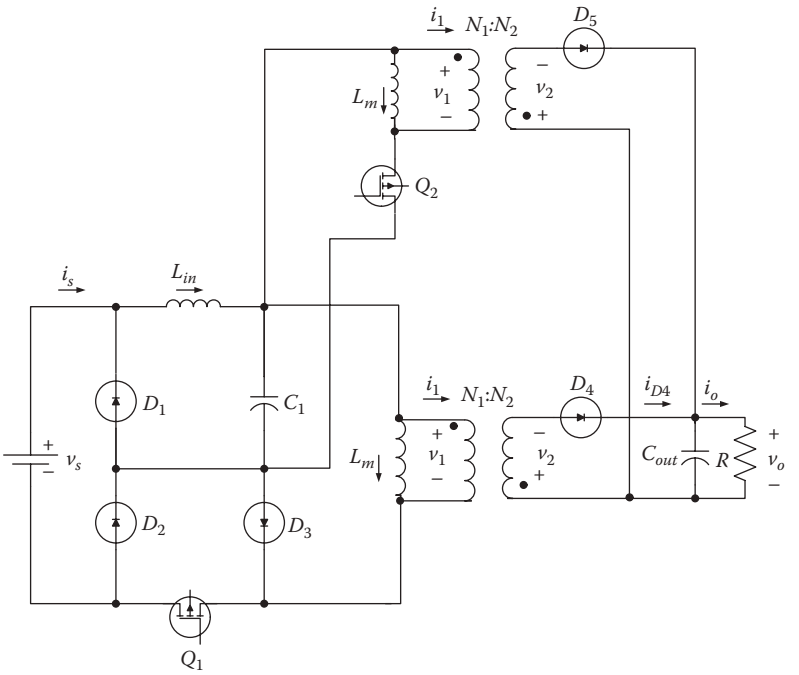


Figure 6.4 Buck parallel flyback converter.

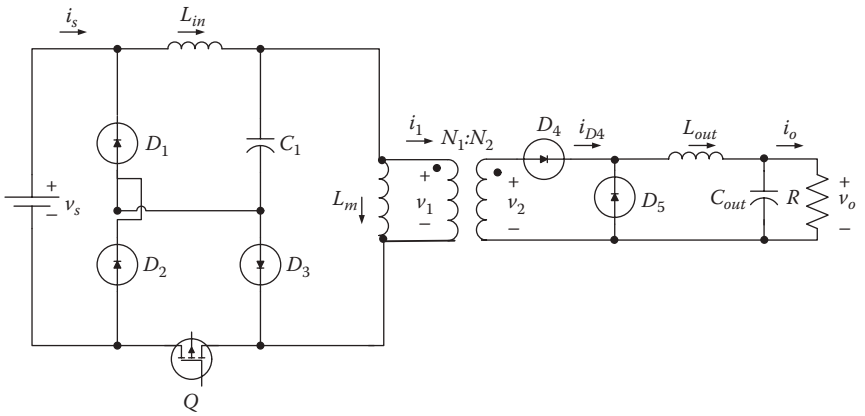


Figure 6.5 Buck forward converter.

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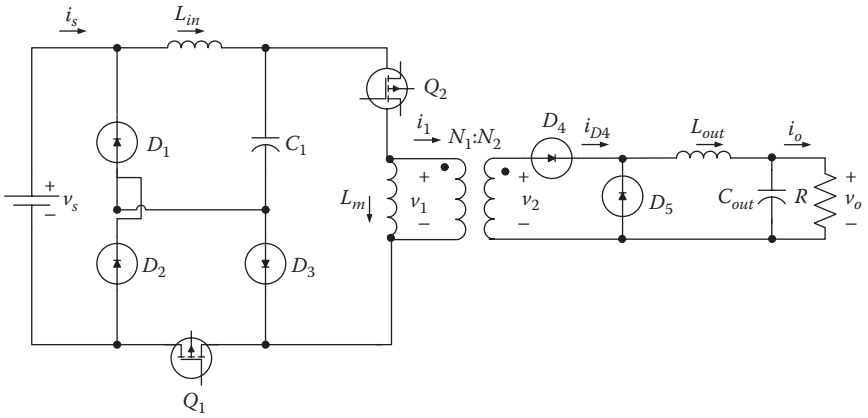


Figure 6.6 Buck double-ended forward converter.

share a common switch Q. The input source V_{c1} for the forward converter is from the output of the boost converter.

6.7 Buck Double-Ended Forward Converter

The buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q_1, capacitor C_1, and input source v_s. It is shown in Figure 6.6.

The double-ended forward converter consists of the capacitor C_1, switch Q_1, switch Q_2, transformer, diode D_3, diode D_4, diode D_5, output inductance L_{out}, output capacitor C_{out}, and load resistor R, where the double-ended forward converter and buck converter share a common switch Q_2. The input source V_{c1} for the double-ended forward converter is from the output of the buck converter [1].

6.8 Buck Series Parallel Forward Converter

The buck series parallel forward converter is shown in Figure 6.7. The buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q_1, capacitor C_1, and input source v_s.

The series parallel forward converter consists of the capacitor C_1, capacitor C_2, switch Q_1, transformer, diode D_1, diode D_2, diode D_3, diode D_4, diode D_5, diode D_6, diode D_7, output inductor L_{out}, output capacitor C_{out}, and load resistor R. The series parallel forward converter and buck converter share a common switch Q_1. The input source V_{c1} and V_{c2} for the series/parallel forward converter is from the output of the buck converter.

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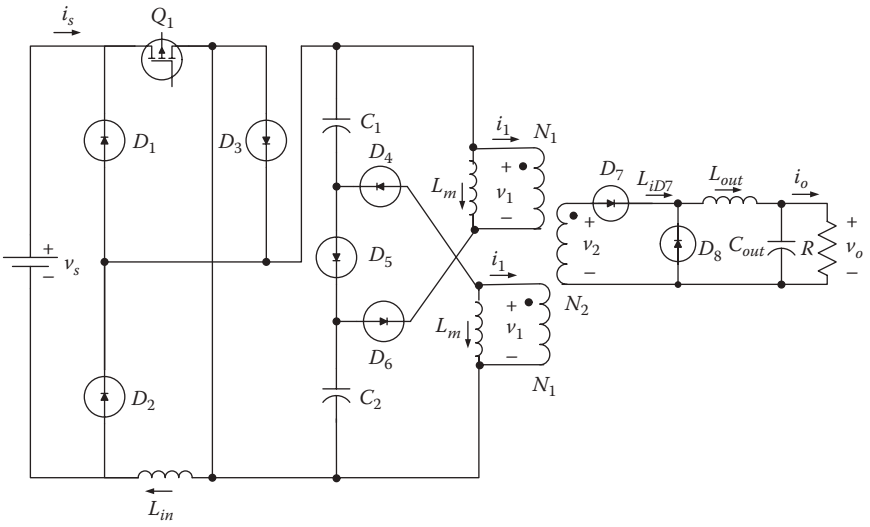


Figure 6.7 Buck series parallel forward converter.

6.9 Buck Parallel Forward Converter

The buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q_1, capacitor C_1, and input source v_s.

The parallel forward converter consists of the capacitor C_1, switch Q_1, switch Q_2, transformers, diode D_3, diode D_4, diode D_5, diode D_6, diode D_7, the output capacitor C_{out}, output inductance L_{out}, and load resistor R, where the parallel forward converter and buck converter share a common switch Q_1. The input source V_{c1} for the parallel forward converter is from the output of the buck converter [1]. This configuration is presented in Figure 6.8.

6.10 Buck Full-Bridge Converter

The buck full-bridge converter is shown in Figure 6.9. The buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q_2, capacitor C_1, and input source v_s.

The full-bridge converter consists of the capacitor C_1, switch Q_1, switch Q_2, switch Q_3, switch Q_4, transformer, diode D_3, diode D_4, diode D_5, diode D_6, output inductance L_{out}, output capacitor C_{out}, and load resistor R, where the full-bridge converter and buck converter share a common switch Q_2. The input source for the full-bridge V_{c1} is from the output of the buck converter.

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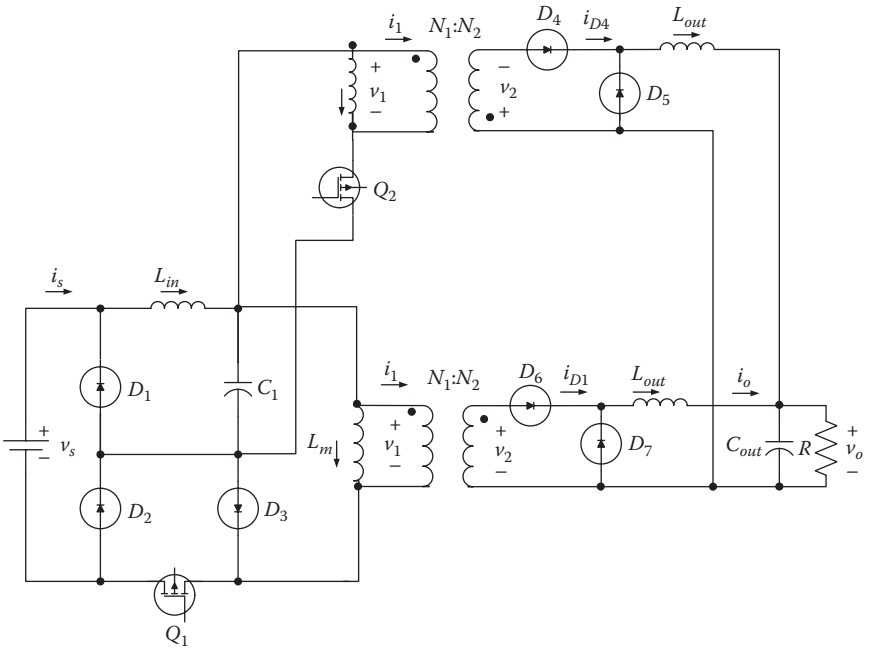


Figure 6.8 Buck parallel forward converter.

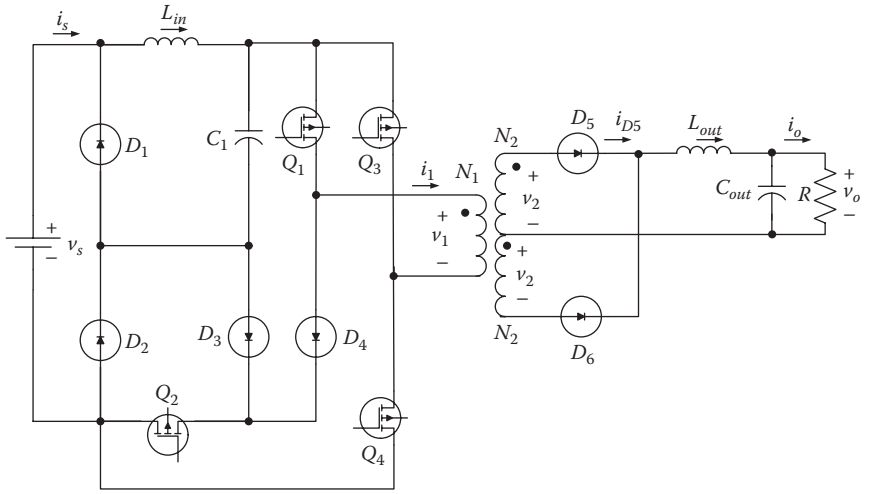


Figure 6.9 Buck full-bridge converter.

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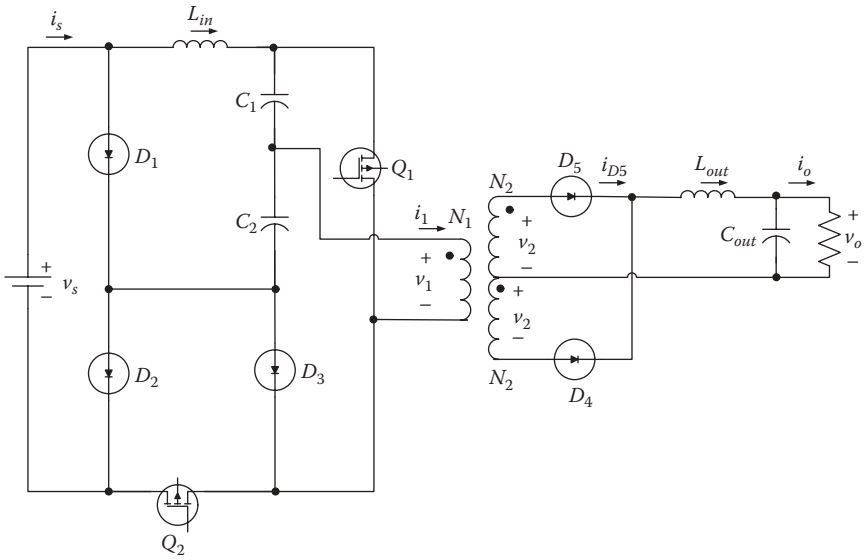


Figure 6.10 Buck half-bridge Converter.

6.11 Buck Half-Bridge Converter

The buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q_2, capacitor C_1, capacitor C_2, and input source v_s, as shown in Figure 6.10.

The half-bridge converter consists of the capacitor C_1, capacitor C_2, switch Q_1, switch Q_2, transformer, diode D_2, diode D_3, diode D_4, output inductance L_{out}, output capacitor C_{out}, and load resistor R, where the half-bridge converter and buck converter share a common switch Q_2. The input source for the half-bridge V_c is from the output of the buck converter.

6.12 Buck Push-Pull Converter

Presented in Figure 6.11, the buck converter consists of inductance L_{in}, diode D_1, diode D_3, switch Q_1, capacitor C_1, and input source v_s.

The push-pull converter consists of the capacitor C_1, switch Q_1, switch Q_2, transformer, diode D_3, diode D_4, diode D_5, output inductance L_{out}, output capacitor C_{out}, and load resistor R, where the push-pull converter and buck converter share a common switch Q_1. The input source for the push-pull V_{c1} is from the output of the buck converter [1].

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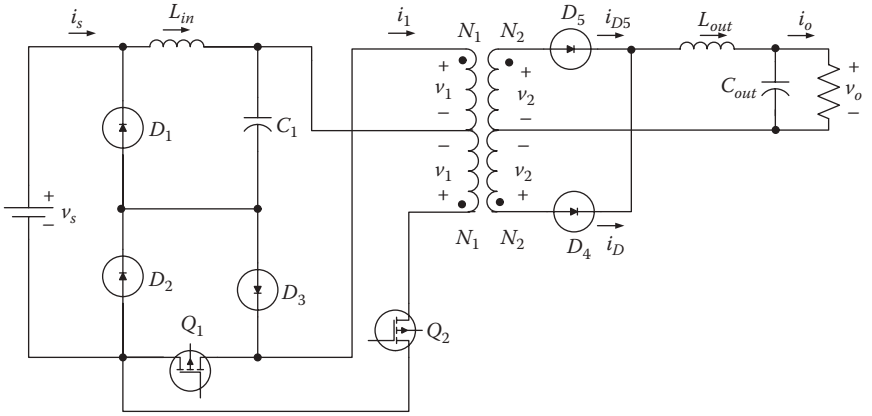


Figure 6.11 Buck push-pull converter.

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chapter eight

Other Types of Integrated Topologies

8.1 Other Types of Integrated Topologies

Other types of integrated converters can be thought of as the parallel construction of two or more basic converters [1]–[9]. We take two basic parallel converters as an example. They share one active switch and one input source voltage.

When the integrated converter works in the fixed switching frequency and duty ratio with the open control loop, the output voltage can be regulated by designing the suitable converter parameters. When it works in the closed control loop, possible control methods can be as follows: (a) by studying converter characteristics, only regulate one of them; (b) alternately regulate two output voltages.

Multi-output voltages can provide custom outputs different output voltages and quality. On the other hand, it increases the density of the converter.

8.2 Buck-Buck Converter

The topology of the buck-buck converter is shown in Figure 8.1. The converters share a common switch Q and input voltage. One buck converter consists of these common components: switch Q, diode D_1, diode D_2, inductor L_{in1}, output capacitor C_{out1}, and resistor R with output voltage v_{o1}. The other buck converter consists of the following common components: switch Q, diode D_3, inductor L_{in2}, output capacitor C_{out2}, and resistor R with output voltage v_{o2}.

8.3 Buck-Buck-Boost Converter

For the buck plus buck-boost double converter, as shown in Figure 8.2, the converters share a common switch Q and input voltage. The buck converter consists of these common components: switch Q, diode D_1, diode D_2, inductor L_{in1}, output capacitor C_{out1}, and resistor R with output voltage v_{o1}. The buck-boost converter consists of the following common components:

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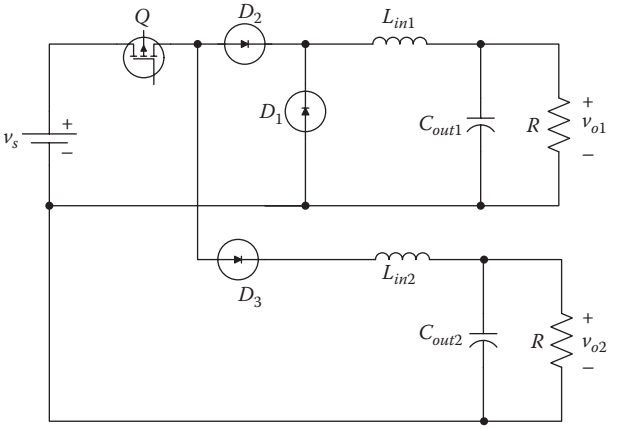


Figure 8.1 Buck-buck converter.

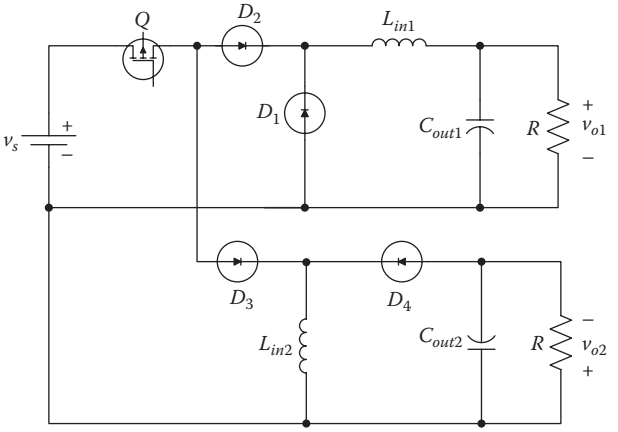


Figure 8.2 Buck-buck boost converter.

switch Q, diode D_3, diode D_4, output capacitor C_{out2}, and resistor R with output voltage v_{o2}.

8.4 Buck-Zeta Converter

For the buck-zeta double arrangement, the converters share a common switch Q and input voltage. The buck consists of common components switch Q, diode D_1, diode D_2, inductor L_{in1}, output capacitor C_{out1}, and resistor R with output voltage v_{o1}. The zeta converter consists of common components switch Q, diode D_3, diode D_4, capacitor C_1, capacitor C_{out2},

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inductor L_{in2}, inductor L_{in3}, resistor R with output voltage v_{o2}. This topology is presented in Figure 8.3.

8.5 Buck-Boost–Buck-Boost Converter

For the buck-boost plus buck-boost double converter, as shown in Figure 8.4, the converters share a common switch Q and input voltage. One buck-boost converter consists of common components switch Q, diode D_1, diode D_2, output capacitor C_{out1}, inductor L_{in1}, and resistor R with output voltage v_{o1}. The other buck-boost converter consists of common

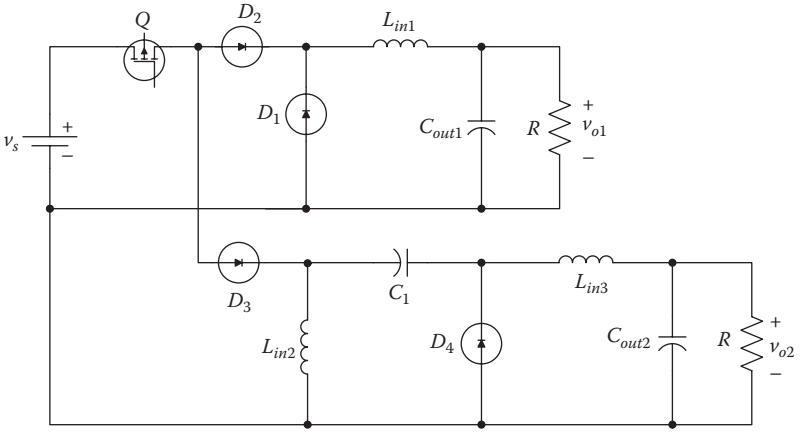


Figure 8.3 Buck-zeta converter.

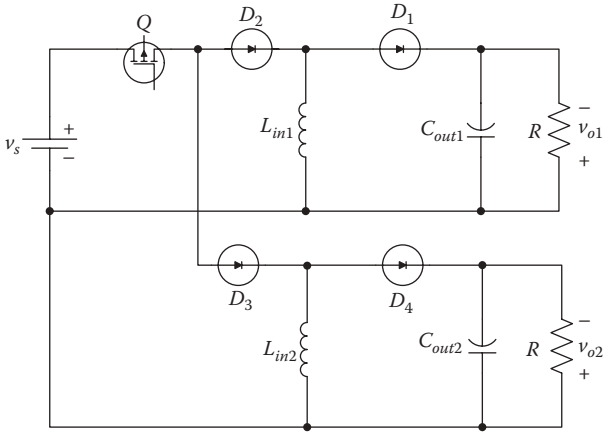


Figure 8.4 Buck-boost–buck-boost converter.

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components switch Q, diode D_3, diode D_4, output capacitor C_{out2}, inductor L_{in2}, and resistor R with output voltage v_{o2}.

8.6 Zeta-Buck-Boost Converter

For the zeta plus buck-boost double converter, the converters share a common switch Q and input voltage. The zeta converter consists of common components switch Q, diode D_1, diode D_2, capacitor C_{out1}, inductor L_{in1}, inductor L_{in2}, and output resistor R with output voltage v_{o1}. The buck-boost converter consists of common components switch Q, diode D_3, diode D_4, capacitor C_{out2}, inductor L_{in2}, and output resistor R with output voltage v_{o2}. This topology is presented in Figure 8.5.

8.7 Zeta-Zeta Converter

The topology of the zeta-zeta converter is shown in Figure 8.6. For the zeta plus zeta double system, the converters share a common switch Q and input voltage. One zeta converter consists of common components diode D_1, diode D_2, capacitor C_1, capacitor C_{out1}, inductor L_{in1}, inductor L_{in2}, and output resistor R with output voltage v_{o1}. The other zeta converter consists of common components diode D_3, diode D_4, capacitor C_2, capacitor C_{out2}, inductor L_{in1}, inductor L_{in2}, and output resistor R with output voltage v_{o2}.

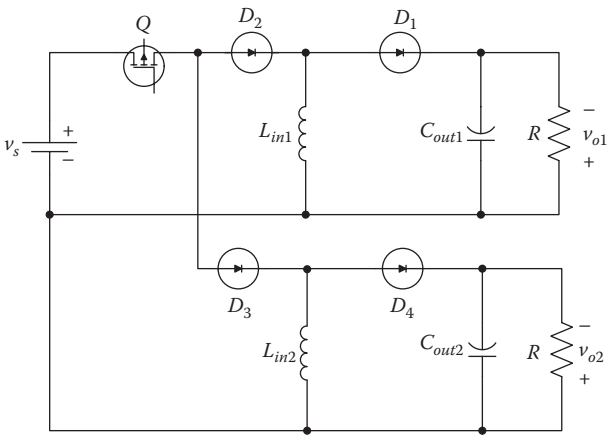


Figure 8.5 Zeta-buck-boost converter.

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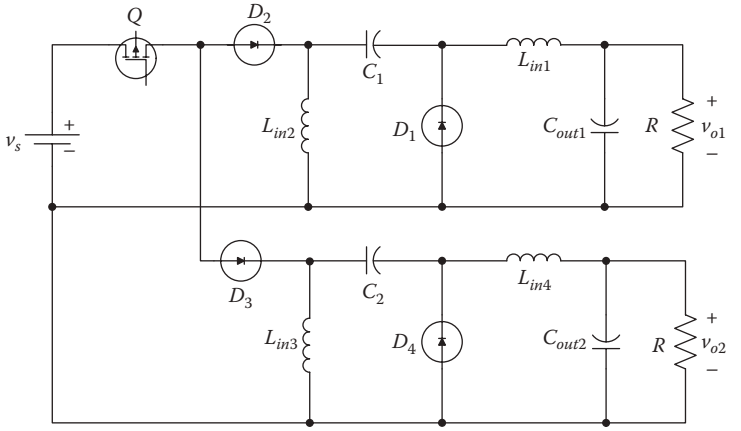


Figure 8.6 Zeta-zeta converter.

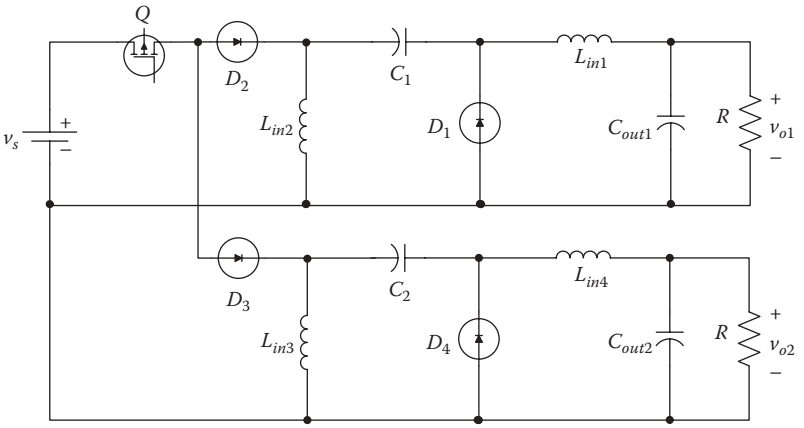


Figure 8.7 Boost-boost converter.

8.8 Boost-Boost Converter

For the boost plus boost double arrangement, (Figure 8.7), the converters share switch Q, and input voltage. One boost converter consists of common components diode D_1, capacitor C_{out1}, and resistor R with output voltage v_{o1}. The other boost converter consists of common components diode D_2, capacitor C_{out2}, and resistor R with output voltage v_{o2}.

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8.9 Boost-Ćuk Converter

For the boost plus Ćuk double converter, shown in Figure 8.8, the converters share common inductor L_{in}, switch Q, and input voltage. The boost converter consists of common components, diode D_1, capacitor C_{out1}, and resistor R with output voltage v_{o1}. The Ćuk converter consists of common components, capacitor C_1, capacitor C_{out2}, diode D_2, inductor L_2, and resistor R with output voltage v_{o2}.

8.10 Boost-SEPIC Converter

For the boost plus SEPIC double converter, shown in Figure 8.9, the converters share common inductor L_{in}, switch Q, and input voltage. The boost

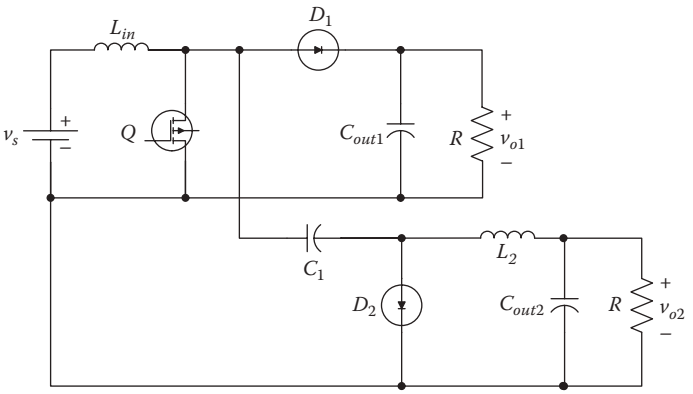


Figure 8.8 Boost-Ćuk converter.

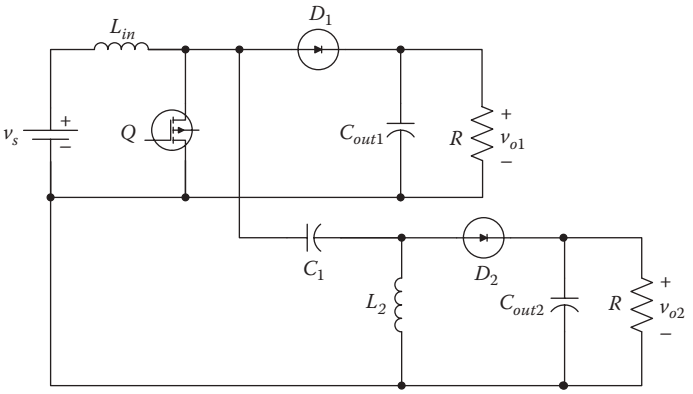


Figure 8.9 Boost-SEPIC converter.

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converter consists of common components diode D_1, capacitor C_{out1}, and resistor R with output voltage v_{o1}. The SEPIC converter consists of common components diode D_2, capacitor C_1, capacitor C_{out2}, inductor L_2, and resistor R with output voltage v_{o2}.

8.11 Ćuk-Ćuk Converter

For the Ćuk plus Ćuk double system (Figure 8.10), the converters share common inductor L_{in}, switch Q, and input voltage. One Ćuk converter consists of components diode D_1, capacitor C_{out1}, and resistor R with output voltage v_{o1}. The other Ćuk converter consists of diode D_2, capacitor C, capacitor C_{out2}, inductor L_2, and resistor R with output voltage v_{o2}.

8.12 SEPIC-Ćuk Converter

For the SEPIC plus Ćuk double system (Figure 8.11), the converters share common inductor L_{in}, switch Q, and input voltage. The SEPIC converter consists of common components diode D_1, capacitor C_2, capacitor C_{out1}, inductor L_1, and output resistor R with output voltage v_{o1}. The Ćuk converter consists of common components diode D_2, capacitor C_1, capacitor C_{out}, inductor L, and resistor R with output voltage v_{o2}.

8.13 SEPIC-SEPIC Converter

For the SEPIC plus SEPIC double system (Figure 8.12), the converters share common inductor L_{in}, switch Q, and input voltage. One SEPIC converter consists of common components diode D_1, capacitor C_2, capacitor C_{out1}, inductor L_1, and resistor R with output voltage v_{o1}. The other SEPIC

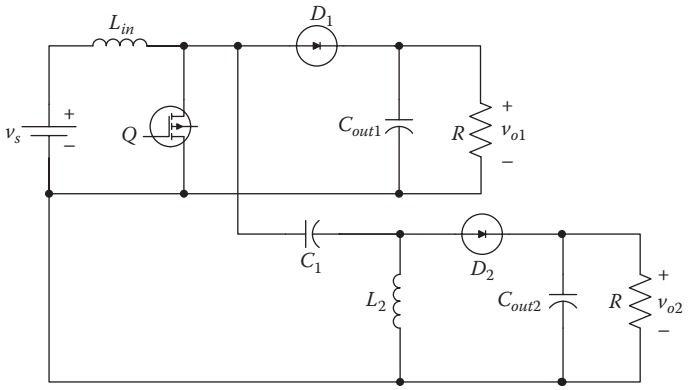


Figure 8.10 Ćuk-Ćuk converter.

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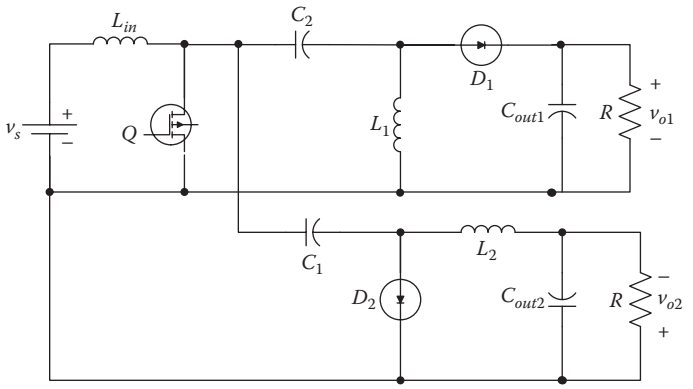


Figure 8.11 SEPIC-Ćuk converter.

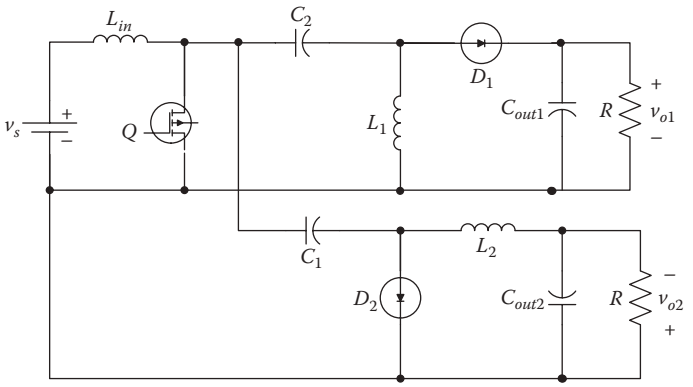


Figure 8.12 SEPIC-SEPIC converter.

converter consists of common components diode D_2, capacitor C_1, capacitor C_{out2}, inductor L_2, and resistor R with output voltage v_{o2}.

8.14 *Flyback Forward Converter*

For the flyback plus forward double system (Figure 8.13), the converters share a common transformer, switch Q, and input voltage. The flyback converter consists of common components diode D_2, capacitor C_{out2}, and resistor R with output voltage v_{o2}. The forward converter consists of components diode D_1, Capacitor C_2, inductor L_1, capacitor C_{out1}, and resistor with output voltage v_{o1}.

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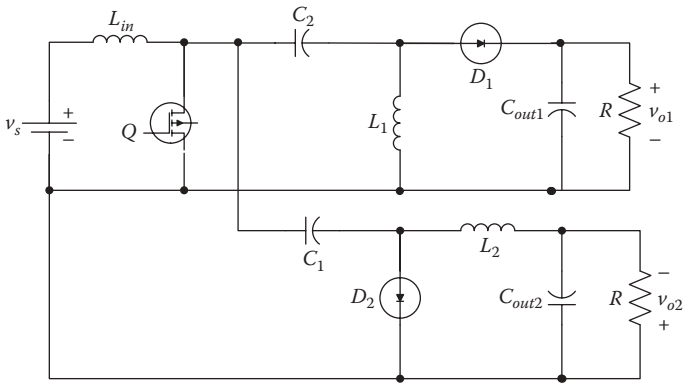


Figure 8.13 Flyback forward converter.

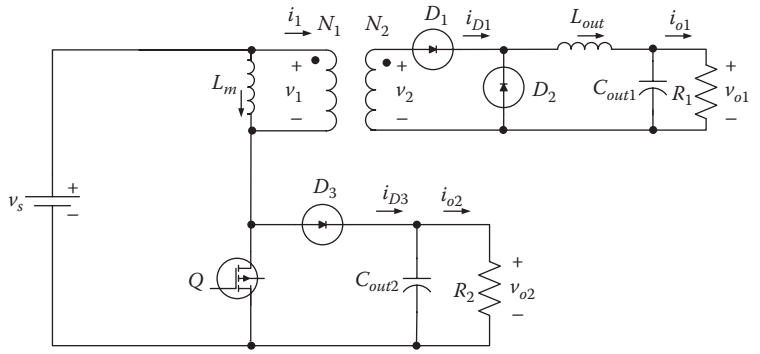


Figure 8.14 Boost-forward converter.

8.15 Boost-Forward Converter

As shown in Figure 8.14, the converters share common inductor L_m, switch Q, and input voltage. The boost converter consists of common components diode D_3, capacitor C_{out2}, and resistor R with output voltage v_{o2}. The forward converter consists of common components diode D_1, diode D_2, transformer, inductor L_{out}, capacitor C_{out1}, and resistor R_1 with output voltage v_{o1}.

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chapter nine

Steady-State Analysis

9.1 Small Ripple Approximation, Inductor Voltage–Second Balance, and Capacitor Charge Balance

9.1.1 Small Ripple Approximation

In practice, the variable of the circuit can be expressed as

$$x(t) = X + x_{ripple}(t), \tag{9.1}$$

This means that the variable consists of the DC component and a small AC component. In any well-designed converter, the ripple is normally required to be less than 1% of the DC component. It is nearly always a good approximation to assume that the magnitude of the ripple is much smaller than the DC component [1]–[4].

$$\left\| x_{ripple}(t) \right\| << X \tag{9.2}$$

Therefore, the variable $x(t)$ is well approximated by its DC component X, with the small ripple term $v_{ripple}(t)$ neglected:

$$x(t) \oplus X \tag{9.3}$$

This approximation is called the small ripple approximation. This method greatly simplifies the analysis of the converter waveforms.

9.1.2 Inductor Voltage–Second Balance Principle

The following equations are applied to inductors:

$$v_l(t) = l\frac{di_l(t)}{dt} \tag{9.4}$$

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where $v_l(t)$ is the inductor voltage, $i_l(t)$ is the inductor current, and l is the value of the inductor.

If integrating the above equation over one switching period, we have:

$$i_l(T) - i_l(0) = \frac{1}{l} \int_0^{T_S} v_l(t)\,dt \tag{9.5}$$

This equation states that the net change in inductor current over one switching period is proportional to the integral of the applied inductor voltage over the interval. In steady state the initial and final value of the inductor current are equal. Hence, in the steady state, the integral of the applied inductor voltage must be zero:

$$0 = \int_0^{T_s} v_l(t)\,dt \tag{9.6}$$

This equation has the units of voltage-seconds. By dividing both sides of the above equation by the switching period T_s,

$$0 = \frac{1}{T_s} \int_0^{T_s} v_l(t)\,dt = \langle v_l \rangle \tag{9.7}$$

This equation states that the average value, or DC component, of the inductor voltage is zero in one switch period in the steady-state condition.

9.1.3 Capacitor Charge Balance Principle

The following equations are applied to capacitors:

$$i_c(t) = c\frac{dv_c(t)}{dt} \tag{9.8}$$

where $v_c(t)$ is the capacitor voltage, $i_c(t)$ is the capacitor current. and c is the value of the capacitor.

If integrating the above equation over one switching period, we have

$$v_c(T) - v_c(0) = \frac{1}{c} \int_0^{T_S} i_c(t)\,dt \tag{9.9}$$

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This equation states that the net change in capacitor voltage over one switching period is proportional to the integral of the applied capacitor current over the interval. In steady state the initial and final values of the capacitor voltages are equal. Hence, in the steady state, the integral of the applied capacitor current must be zero:

$$0 = \int_0^{T_s} i_c(t)\,dt \tag{9.10}$$

This equation has the units of ampere-seconds. By dividing both sides of the above equation by the switching period T_s,

$$0 = \frac{1}{T_s}\int_0^{T_s} i_c(t)\,dt = \langle i_c \rangle \tag{9.11}$$

This equation states that the average value, or DC component, of the capacitor current is zero in one switch period in the steady-state condition.

9.2 BIFRED Converter Example

Figure 9.1 depicts BIFRED topology with the above methods.

When the BIFRED converter is in mode 1 (CCM-CCM), circuits for on-time and off-time intervals are as depicted in Figure 9.2. Note that CCM/DCM-CCM/DCM is classified by the current waveforms of i_{in} & i_m [5]–[11].

When the BIFRED converter is in mode 2 (CCM-DCM) and the switch is on, the circuit has the configuration shown in Figure 9.3(a). When the switch is off, the circuits are as depicted in Figure 9.3(b).

When the BIFRED converter is in mode 3 (DCM-CCM) and the switch is on, the circuit has the configuration shown in Figure 9.2(a). When the switch is off, the circuit at the first stage is as shown in Figure 9.3(a). After this time interval, the circuit is depicted as shown in Figure 9.4.

When the BIFRED converter is in mode 4 (DCM-DCM with $D1 < D2$) and the switch is on, the circuit has the configuration shown in Figure 9.2(a). When the switch is off, the circuit at the first stage is as depicted in Figure 9.3(a); at the second stage, it is as shown in Figure 9.4. Then, the circuit is as depicted in Figure 9.5.

When the BIFRED converter is in mode 5 (DCM-DCM with $D2 < D1$), the circuits have the same waveforms as the BIFRED converter in mode 2.

The following illustrates current waveforms of BIFRED converters in different modes of operation. When the BIFRED converter is in mode 1, current waveforms for l_m, l_{in} are as presented in Figure 9.6.

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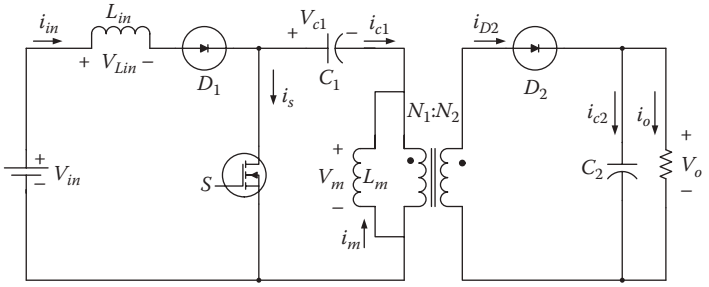


Figure 9.1 Isolated BIFRED converter (practical transformer).

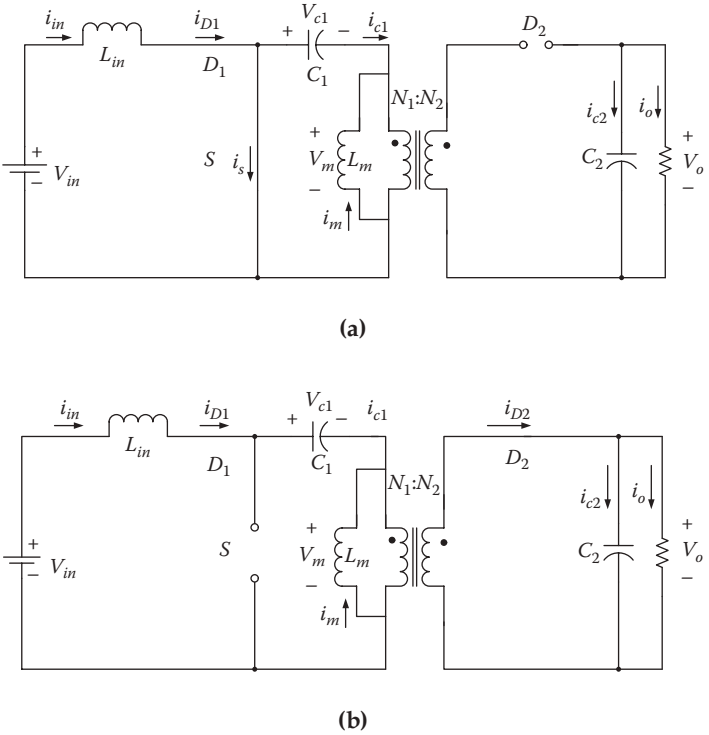


Figure 9.2 Isolated BIFRED converter in mode 1.

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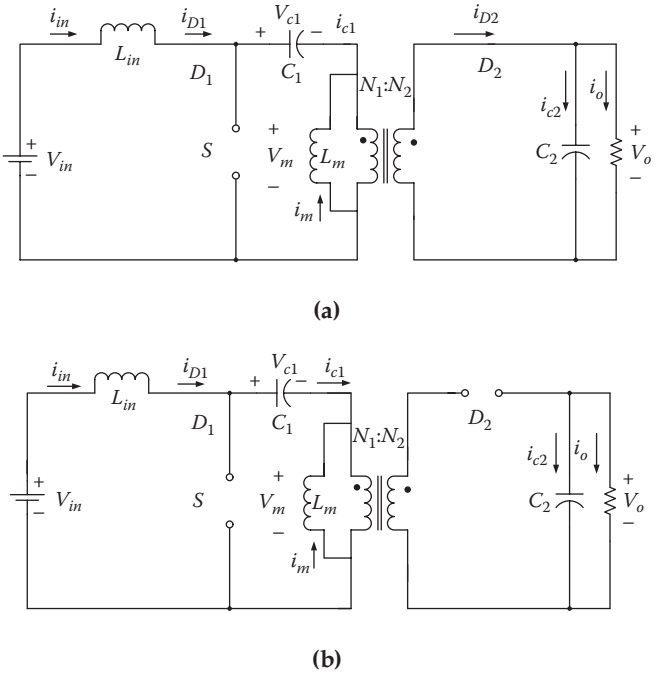


Figure 9.3 Isolated BIFRED converter in mode 2.

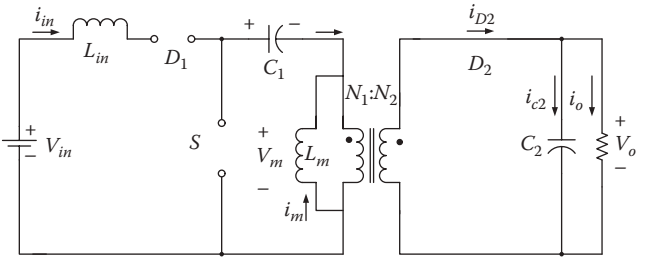


Figure 9.4 Isolated BIFRED converter in mode 3 during $(1 - D - \Delta_1)T$, $\Delta_1 < \Delta_2$, switch: off.

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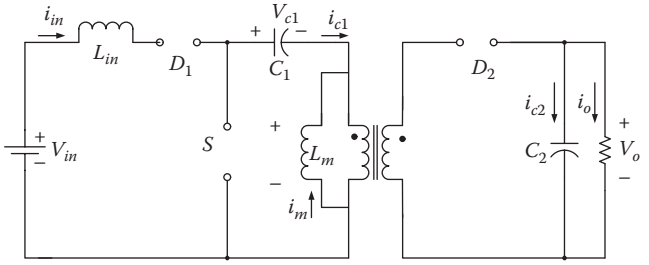


Figure 9.5 Isolated BIFRED converter in mode 4 during $(1 - D - \Delta_2)T$, $\Delta_1 < \Delta_2$, switch: off.

When the BIFRED converter is in mode 2, current waveforms of l_m, l_{in} are as depicted in Figure 9.7.

When the BIFRED converter is in mode 3 (DCM-CCM), current waveforms of l_m, l_{in} are as depicted in Figure 9.8.

When the BIFRED converter is in mode 4 (DCM-DCM), current waveforms of l_m, l_{in} are as depicted in Figure 9.9.

When the BIFRED converter is in mode 1, the DC voltage conversion ratio in mode 1, m_1, can be obtained by the following:

$$m_1 = \frac{v_o}{v_{in}} = \frac{nD}{1 - D} \tag{9.12}$$

where $n = n_2 / n_1$. In mode 5, the DC voltage conversion ratio, m_2, can be obtained as Equation (9.13).

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T}$$

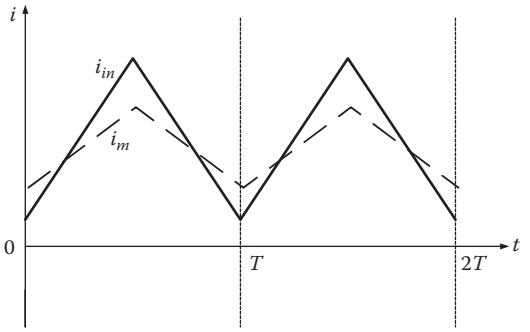
When the BIFRED converter is in mode 2,

$$m_2 = \frac{v_o}{v_{in}} = \frac{nD}{\mathrm{D}} = \frac{D}{\sqrt{k}} \tag{9.13}$$

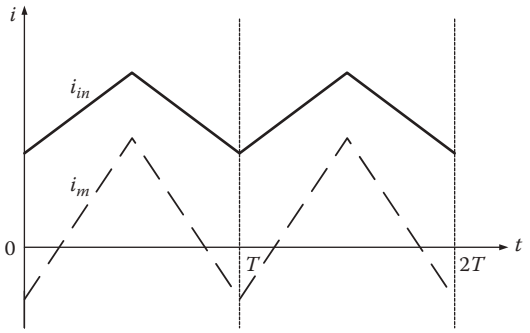
where $k = 2l_{in} \cdot l_m / rT(l_{in} + l_m)$, $D = t_{on} / (t_{on} + t_{off}) = t_{on} / T$.

When the BIFRED converter is in mode 3, the DC voltage conversion ratio, m_3, can be obtained by the following:

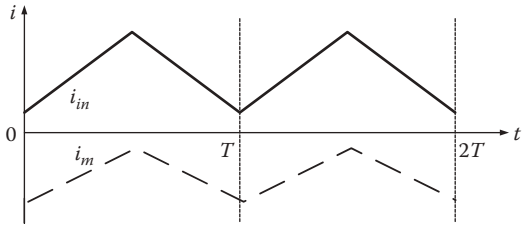
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(a) BIFRED in CCM-CCM with ($0 < i_{m,min}, 0 < i_{in,min}, k_c < k$)



(b) BIFRED in CCM-CCM with ($i_{im,min} < 0 < i_{im,max}, 0 < i_{in,min}, k_c < k$)



(c) BIFRED in CCM-CCM with ($i_{m,max} < 0, 0 < i_{in,min}, k_c < k$)

Figure 9.6 Current waveform of BIFRED converter in mode 1.

$$m_3 = \frac{v_o}{v_{in}} = \frac{n(D + D_1)}{D_1} D = nD\left(1 + \frac{RT}{n^2\left(l_{in} + \sqrt{l_{in}^2 + \frac{2TRl_{in}}{n^2}}\right)}\right) \tag{9.14}$$

When the BIFRED converter is in mode 4, the DC voltage conversion ratio, m_4, can be obtained by the following:

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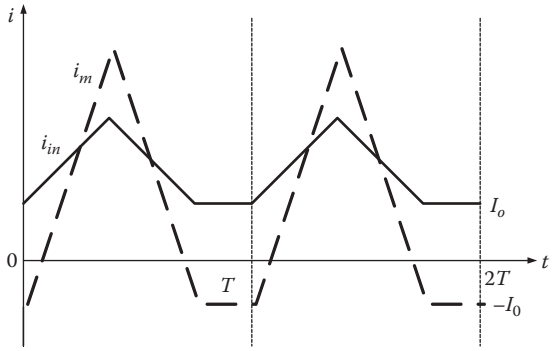


Figure 9.7 Current waveform of BIFRED converter in mode 2, CCM-DCM.

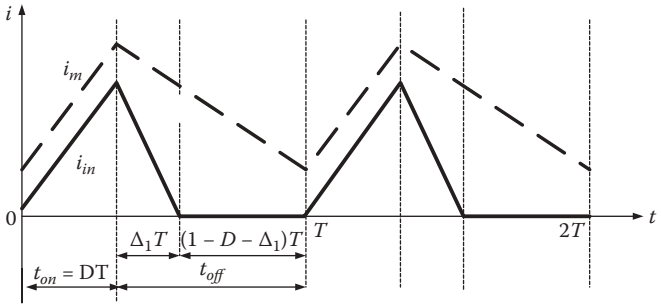


Figure 9.8 Current waveform of BIFRED converter in mode 3.

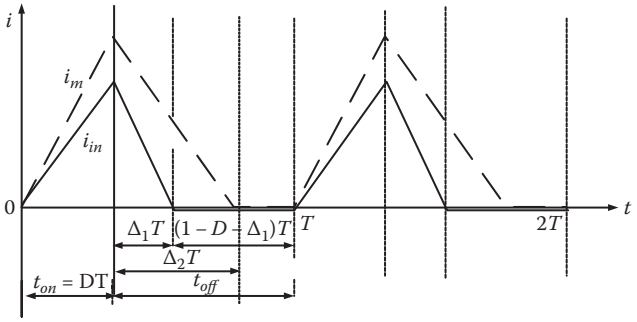


Figure 9.9 Current waveform of BIFRED converter in mode 4.

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$$\left(\frac{2l_{in}m_4^2}{RTD^2}-1\right)\left(\frac{m_4}{2n}\sqrt{1+\frac{8l_m n^2}{RTD^2}}+\frac{m_4}{2n}-1\right)=1 \tag{9.15}$$

When $k > k_c$, the BIFRED converter is in mode 1 and when $k < k_c$, the BIFRED converter is in other modes. When the BIFRED converter is in mode 3 and mode 4, and if the diode D_1 is taken away, the current waveform will be the same as that in the SEPIC converter. Therefore, the condition for BIFRED converters in mode 3 is

$$i_{in,\min} < 0 < i_{in,\max} \tag{9.16}$$

$$0 < i_{m,\min} \tag{9.17}$$

$$k < k_c \tag{9.18}$$

$$l_m > l_{m0} \tag{9.19}$$

In addition, the condition for the BIFRED converter in mode 4 is

$$i_{in,\min} < 0 < i_{in,\max} \tag{9.20}$$

$$0 < i_{m,\min} \tag{9.21}$$

$$k < k_c \tag{9.22}$$

$$l_m < l_{m0} \tag{9.23}$$

When the BIFRED converter is in mode 2 and mode 5, and if diode D_1 is taken away, the current waveform will be the same as that in the SEPIC converter. The condition for the BIFRED converter in mode 2 is

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$$i_{m,\min} < 0 < i_{m,\max} \tag{9.24}$$

$$0 < i_{in,\min} \tag{9.25}$$

$$k < k_c \tag{9.26}$$

$$l_n > l_{n0} \tag{9.27}$$

In addition, the condition for the BIFRED converter in mode 5 is

$$i_{m,\min} < 0 < i_{m,\max} \tag{9.28}$$

$$0 < i_{in,\min} \tag{9.29}$$

$$k < k_c \tag{9.30}$$

$$l_n < l_{n0} \tag{9.31}$$

As a result, for mode 1:

$$i_{in,\min} = \left(\frac{nD}{1-D}\right)^2 \frac{1}{r} v_{in} - \frac{v_{in} DT}{2 l_{lin}} \tag{9.32}$$

$$i_{in,\max} = \left(\frac{nD}{1-D}\right)^2 \frac{1}{r} v_{in} + \frac{v_{in} DT}{2 l_{lin}} \tag{9.33}$$

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$$i_{m,\min} = \frac{nDv_{in}}{(1-D)r} - \frac{v_{in}DT}{2l_m} \tag{9.34}$$

$$i_{m,\max} = \frac{nDv_{in}}{(1-D)r} + \frac{v_{in}DT}{2l_m} \tag{9.35}$$

For other modes:

$$i_{in,\min} = \frac{D^2 v_{in}}{RK} - \frac{DTv_{in}}{2l_{in}}(D + \frac{nD}{m}) = \frac{v_{in}D^2T}{2l_{in}}(\frac{l_n}{l_m} - \frac{n}{m}) \tag{9.36}$$

$$i_{in,\max} = i_{in,\min} + \frac{v_{in}DT}{l_{in}} = \frac{v_{in}DT}{2l_{lin}}(D\frac{l_n}{l_m} - D\frac{n}{m} + 2) \tag{9.37}$$

$$i_{m,\min} = i_{m,average} - \frac{v_{in}DT\left(D+\mathrm{D}\right)}{2l_m} = D\sqrt{T}v_{in}(n\sqrt{\frac{l_m + l_n}{2Rl_m l_n}} - \frac{D\sqrt{T}}{2l_m}(1+\frac{n}{m})) \tag{9.38}$$

$$i_{m,\max} = i_{m,\min} + \frac{v_{in}DT}{l_m} = D\sqrt{T}v_{in}(n\sqrt{\frac{l_m + l_n}{2Rl_m l_n}} - \frac{D\sqrt{T}}{2l_m}(1+\frac{n}{m}) + \frac{\sqrt{T}}{l_m}) \tag{9.39}$$

We can get the boundary value l_{in} for the BIFRED converter in mode 1 and mode 3 as the following:

$$l_{in0} = \frac{\left(1-D\right)^2 TR}{2n^2 D} \tag{9.40}$$

And the boundary value of l_m for the BIFRED converter in mode 2 and mode 4 is

$$l_{m0} = \frac{\left(1-D\right)TR}{2n^2} \tag{9.41}$$

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chapter ten

Dynamic Analysis

10.1 Methodology

In order to study the dynamic characteristic of the integrated converter, some models and assumptions will be needed [1]–[4]. First, average variable value will be thought of as the sum of steady state value and small perturbation variable value [4], [5]. Second, higher order small perturbation will be ignored in the final model and calculation. Finally, the DC transfer model is used for the small signal model. The small signal model for the buck integrated forward converter in a different model will be derived in the following section [2].

10.2 Buck Integrated Forward Converter Example

The topology of the buck integrated forward converter is shown in Figure 10.1. The buck converter consists of inductor L_{in}, diode D_1, diode D_3, switch Q, capacitor C_1, and input source v_s. The forward converter consists of capacitor C_1, switch Q, transformer, diode D_3, diode D_4, diode D_5, output capacitor C_{out}, output inductor L_{out}, and load resistor R. In the buck integrated forward converter, the buck converter and forward converter share a common switch Q. The input source V_{c1} for the forward converter is from the output of the boost converter. In order to reset the transformer winding during every period, the maximum duty for this buck integrated forward converter is less than 0.5.

When switch Q is on, capacitor C_1 discharges through the transformer, switch Q, and diode D_2 for supplying, together with current $i_{Lin,}$ the forward converter. At the same time, input voltage charges the capacitor C_1 by inductor L_{in}, capacitor C_1, diode D_3, and switch Q. When the switch is off, the current on the inductor L_{in} can be continuous and discontinues. So does the current on the output inductor L_{out}. According to different combinations of operation modes, there are five operation modes for the circuit: CCM-CCM, CCM-DCM, DCM-CCM, DCM-DCM1, and DCM-DCM2. i_{Lm} is always in discontinuous conduction mode.

When both buck and forward converter operate in CCM mode with switch on ($0 < t < DT$) (Figure 10.2), the formulations are as follows:

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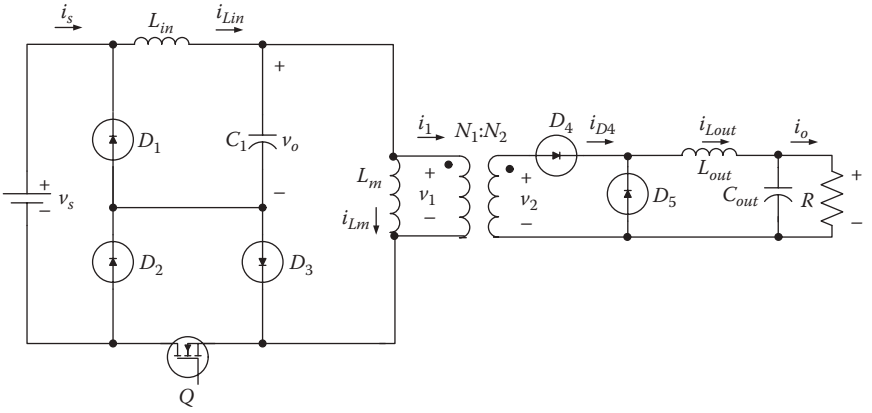


Figure 10.1 Buck integrated forward converter.

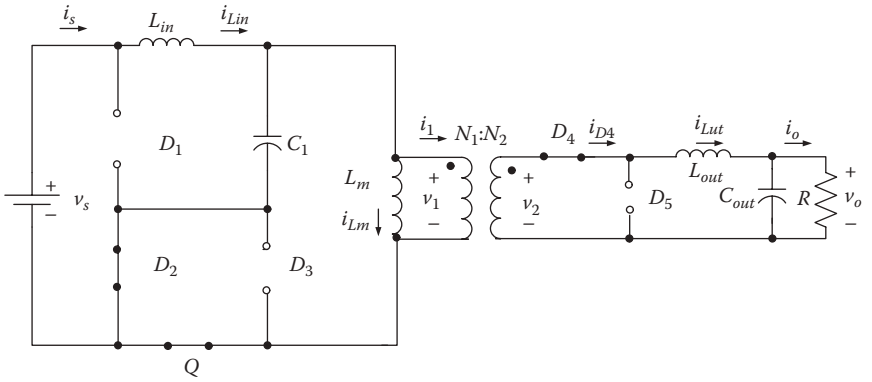


Figure 10.2 Buck integrated forward converter (during DT, switch: on).

$$V_s = v_{Lin} + V_{c1} \tag{10.1}$$

$$\frac{di_{Lin}}{dt} = \frac{V_s - V_{c1}}{L_{in}} \tag{10.2}$$

$$i_{Lin}(t) = \frac{V_s - V_{c1}}{L_{in}} t + I_{Lin,\min} \tag{10.3}$$

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$$i_{Lin}(t = DT) = I_{Lin,\max} \tag{10.4}$$

$$I_{Lin} = I_{Lin,\max} - I_{Lin,\min} = \frac{V_s - V_{c1}}{L_{in}} DT \tag{10.5}$$

When the switch is off ($DT < t < T$) (Figure 10.3),

$$v_{Lin} = -V_{c1} \tag{10.6}$$

$$\frac{di_{Lin}}{dt} = \frac{-V_{c1}}{L_{in}} \tag{10.7}$$

$$i_{Lin}(t) = \frac{-V_{c1}}{L_{in}}\left(t - DT\right) + I_{Lin,\max} \tag{10.8}$$

$$i_{Lin}(t = T) = I_{Lin,\min} \tag{10.9}$$

$$I_{Lin} = I_{Lin,\max} - I_{Lin,\min} = \frac{V_{c1}}{L_{in}}\left(1 - D\right)T \tag{10.10}$$

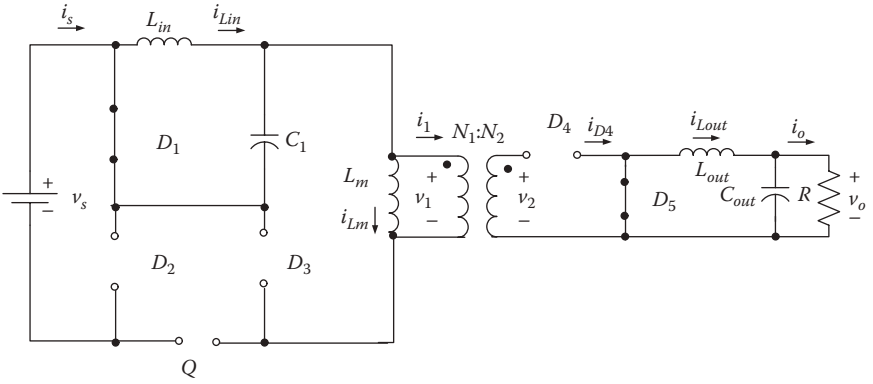


Figure 10.3 Buck integrated forward converter (during (1-D) T, switch: off).

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Thus (Figure 10.4),

$$\frac{V_s - V_{c1}}{L_{in}} DT = \frac{V_{c1}}{L_{in}}(1-D)T \tag{10.11}$$

Thus, the voltage ratio for the buck converter is

$$V_{c1} = DV_s \tag{10.12}$$

In the same way, the voltage ratio for the forward converter is

$$\frac{V_o}{V_{C1}} = \frac{N_2}{N_1} D, \tag{10.13}$$

where D is the duty for both converter and the maximum value for D should be less than 0.5 for the purpose of resetting the forward converter. Thus, the voltage ratio for the buck integrated forward converter is

$$\frac{V_o}{V_s} = \frac{N_2}{N_1} D^2 \tag{10.14}$$

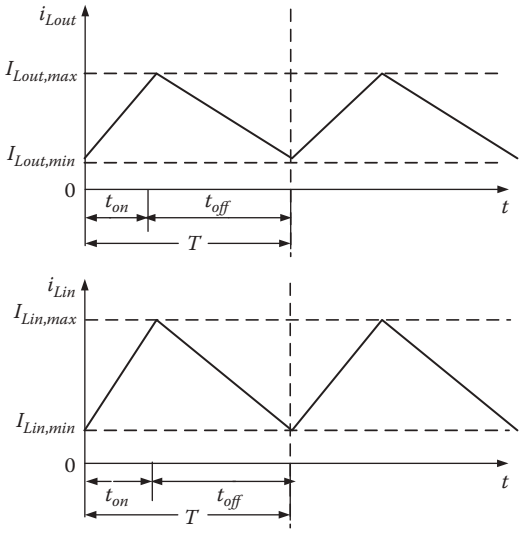


Figure 10.4 Current waveforms for input inductor and output inductor in CCM-CCM.

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The boundary conditions between continuous and discontinuous conduction:

$$I_{Lin} = \frac{V_{c1}}{L_{in}}(1 - \frac{V_{c1}}{V_s})T \tag{10.15}$$

$$I_{Lin} = I_o = \frac{V_{c1}}{R} \tag{10.16}$$

$$I_{Lin,\min} = I_{Lin} - \frac{\Delta I_{Lin}}{2} = \frac{V_{c1}}{R} - \frac{V_{c1}}{2L}\left(1 - \frac{V_{c1}}{V_s}\right)T = V_{c1}\left(\frac{1}{R} - \frac{\left(V_s - V_{c1}\right)}{2L_{in}fV_s}\right) \tag{10.17}$$

$$I_{Lin,\min} = 0 \qquad \frac{1}{R} - \frac{\left(V_s - V_{c1}\right)}{2L_{in}fV_s} = 0 \tag{10.18}$$

$$L_{in,\min} = \frac{\left(V_s - V_{c1}\right)R}{2fV_s} = \frac{\left(1 - D\right)R}{2f} \tag{10.19}$$

Minimum C required for the specific output voltage ripple:

$$i_{c1} = C_1 \frac{dv_{c1}}{dt} \tag{10.20}$$

$$\Delta V_{c1} = \frac{1}{C_1}\int_{t1}^{t2} i_{c1}dt = \frac{1}{C_1}\Delta Q = \frac{1}{C_1}\frac{1}{2}\frac{T}{2}\frac{\Delta I_{Lin}}{2} \tag{10.21}$$

$$\Delta V_{c1} = \frac{1}{8C_1 f}\left(\frac{V_{c1}}{L_{in}}\right)\left(1 - D\right)T \tag{10.22}$$

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$$\Delta V_{c1} = \frac{(1 - D)V_{c1}}{8 L_{in} C_1 f^2} \tag{10.23}$$

$$\frac{\Delta V_{c1}}{V_{c1}} = \frac{(1 - D)}{8 L_{in} C_1 f^2} \tag{10.24}$$

When the buck converter operates in CCM and the forward converter operates in DCM, the voltage ratio for the buck converter is

$$\frac{V_{C1}}{V_s} = D \tag{10.25}$$

For the forward converter, when the switch Q is on (Figure 10.5), the voltage on the inductor L_{out} is

$$V_{Lm} = \frac{N_2}{N_1} V_{C1} - V_o \tag{10.26}$$

When the switch Q is off (Figures 10.6 and 10.7), the voltage on the inductor L_{out} is

$$V_{Lm} = V_o \tag{10.27}$$

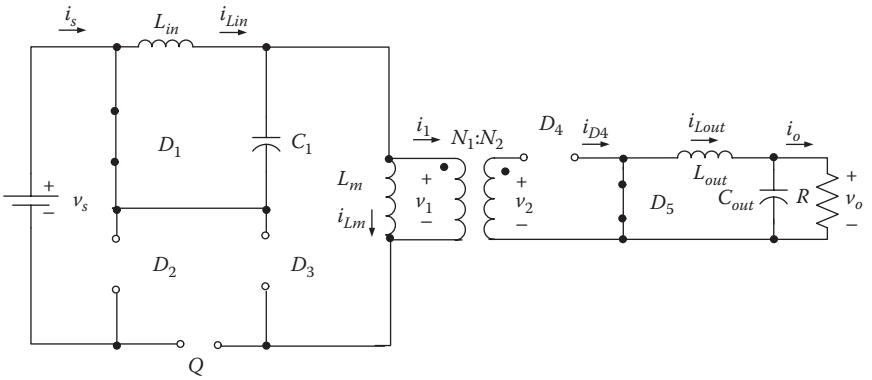


Figure 10.5 Buck integrated forward converter (during DT, switch: on).

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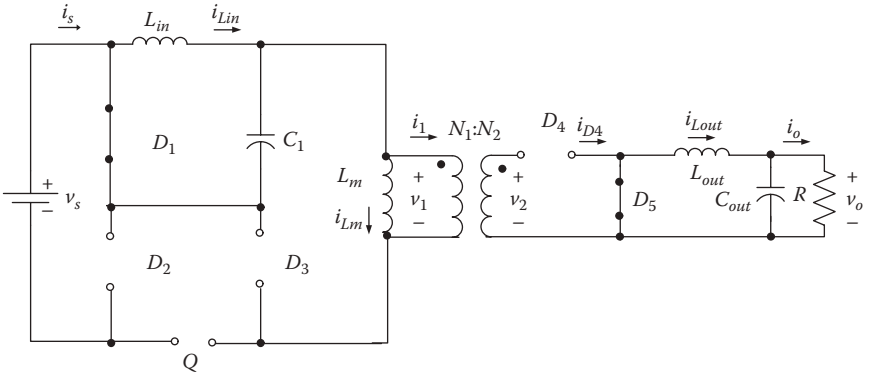


Figure 10.6 Buck integrated forward converter (during T, switch: off).

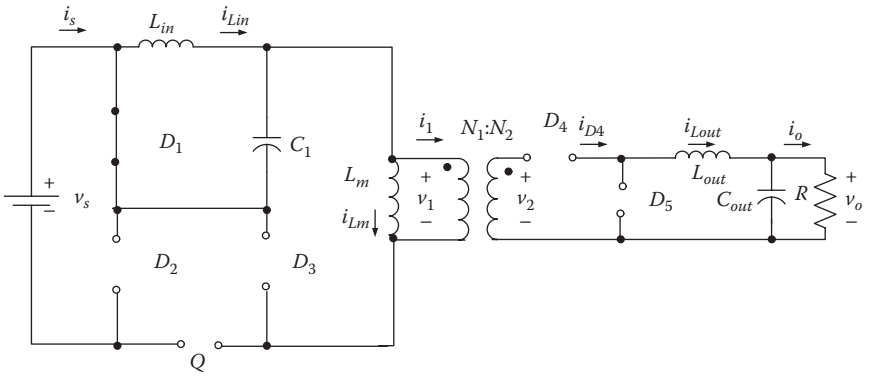


Figure 10.7 Buck integrated forward converter (during (1–D–Δ) T, switch: off).

When the inductor L_{out} works in CCM, the integral of voltage in a switch period T should be zero. Thus,

$$(\frac{N_2}{N_1} V_{C1} - V_o)DT - V_o(1-D)T = 0 \tag{10.28}$$

$$\frac{V_o}{V_{C1}} = \frac{N_2}{N_1} D \tag{10.29}$$

When the inductor L_{out} works in DCM, the integral of voltage in a switch period T should be zero. Hence,

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$$(\frac{N_2}{N_1}V_{c1} - V_o)DT - V_o \quad T = 0 \tag{10.30}$$

$$\frac{V_o}{V_{C1}} = \frac{D}{D+}\frac{N_2}{N_1} = \frac{N_2}{N_1}\frac{D}{\left(D+\right)} \tag{10.31}$$

where we have

$$\mathrm{D} = \frac{-D+\sqrt{D^2+\frac{8L_{out}}{RT}}}{2} \tag{10.32}$$

So, we can determine the voltage ratio for the buck integrated forward converter in CCM-DCM mode (Figure 10.8):

$$\frac{V_o}{V_s} = \frac{N_2}{N_1}\frac{2D^2}{D+\sqrt{D^2+\frac{8L_{out}}{RT}}} \tag{10.33}$$

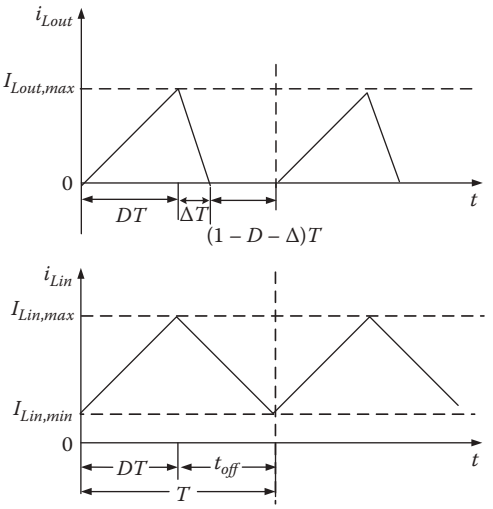


Figure 10.8 Current waveforms for input inductor and output inductor in CCM-DCM.

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In DCM plus CCM mode, in the buck integrated forward converter, the buck operates in DCM and the forward operates in CCM.

For the buck converter, when the switch is on ($0 < t < DT$) (Figure 10.9),

$$\frac{di_{Lin}}{dt} = \frac{V_s - V_{c1}}{L_{in}} \tag{10.34}$$

$$i_{Lin}(t = DT) = I_{Lin,\max} = \frac{V_s - V_{c1}}{L_{in}} DT \tag{10.35}$$

When the switch is off ($DT < t < (D + \mathrm{D})T$) (Figures 10.10 and 10.11),

$$i_{Lin}(t) = \frac{-V_{c1}}{L_{in}}\left(t - DT\right) + I_{Lin,\max} \tag{10.36}$$

$$i_{Lin}(t = (D + \mathrm{D})T) = 0 \tag{10.37}$$

Thus, the voltage ratio for the DCM buck converter is

$$\frac{V_{c1}}{V_s} = \frac{D}{D + \mathrm{D}} \tag{10.38}$$

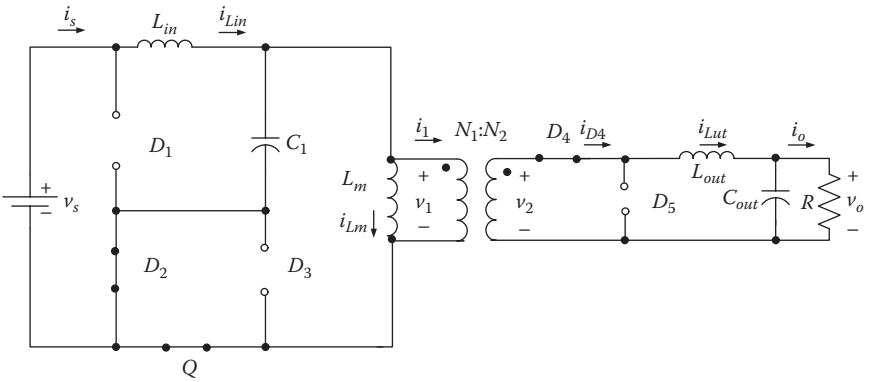


Figure 10.9 Buck integrated forward converter (during DT, switch: on).

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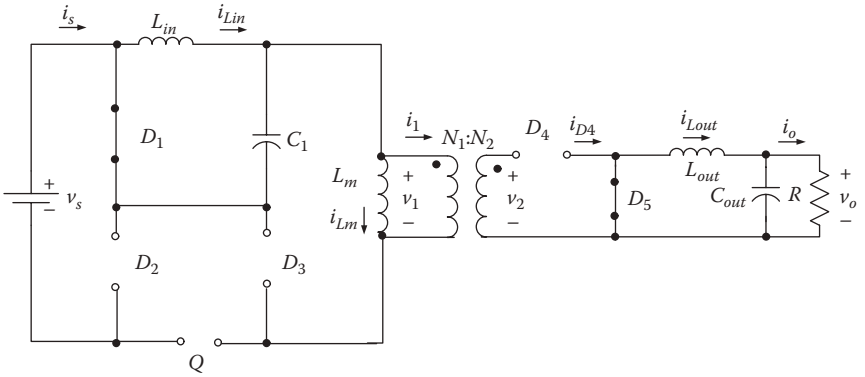


Figure 10.10 Buck integrated forward converter (during Δ T, switch: off)

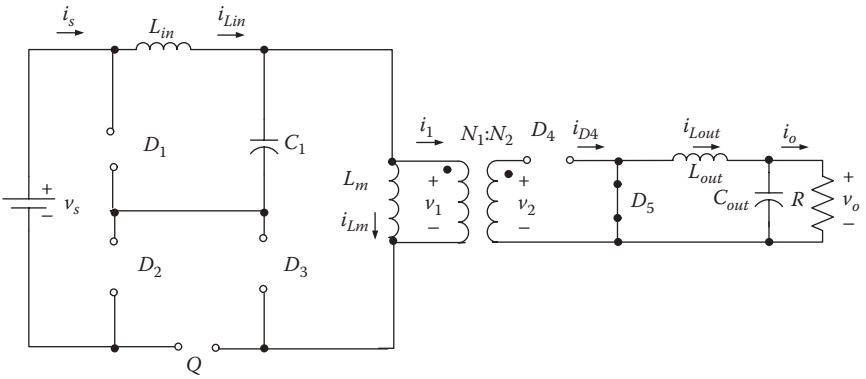


Figure 10.11 Buck integrated forward converter (during (1–D–Δ) T, switch: off).

where

$$D = \frac{-D + \sqrt{D^2 + \dfrac{8L_{in}}{R_e T}}}{2} \tag{10.39}$$

$$R_e = \left(\frac{N_1}{N_2 D}\right)^2 R \tag{10.40}$$

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Thus,

$$\frac{V_{c1}}{V_s} = \frac{2D}{D + \sqrt{D^2 + \dfrac{8L_{in}}{R_e T}}} \tag{10.41}$$

The voltage ratio for the forward converter is

$$\frac{V_o}{V_{C1}} = \frac{N_2}{N_1} nD \tag{10.42}$$

Thus, we can have the voltage ratio for the buck integrated forward converter in DCM-CCM mode (Figure 10.12):

$$\frac{V_o}{V_s} = \frac{N_2}{N_1} \frac{2D}{1 + \sqrt{1 + \dfrac{8L_{in}}{RT} \dfrac{N_2{}^2 D^2}{N_1{}^2}}} \tag{10.43}$$

The voltage ratio for the DCM buck converter is

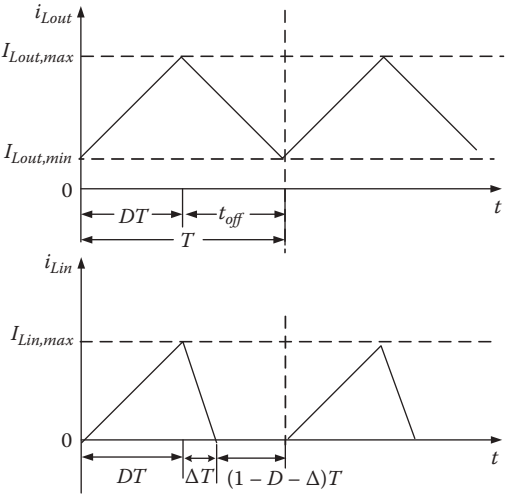


Figure 10.12 Current waveforms for input inductor and output inductor in DCM-CCM.

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$$\frac{V_{c1}}{V_s} = \frac{D}{D + \Delta_1} \tag{10.44}$$

where

$$\Delta_1 = \frac{-D + \sqrt{D^2 + \frac{8L_{in}}{R_e T}}}{2} \tag{10.45}$$

$$R_e = \frac{V_{c1}^2}{P} \tag{10.46}$$

The voltage ratio for the DCM forward converter is

$$\frac{V_o}{V_{c1}} = \frac{D}{D + \Delta_2} \tag{10.47}$$

where

$$\Delta_2 = \frac{-D + \sqrt{D^2 + \frac{8L_{out}}{RT}}}{2} \tag{10.48}$$

So, for buck integrated forward converter in DCM-DCM, the voltage ratio is

$$\frac{V_o}{V_s} = \frac{D^2}{(D + \Delta_1)(D + \Delta_2)} \tag{10.49}$$

In DCM-DCM ($\Delta_1 > \Delta_2$) mode, both buck converter and forward converter operate in DCM mode for the input inductor L_{in} and output inductor L_{out}. Two kinds of DCM modes are classified by the different times of inductors reaching the zero current after switch is off (Figures 10.13–10.17).

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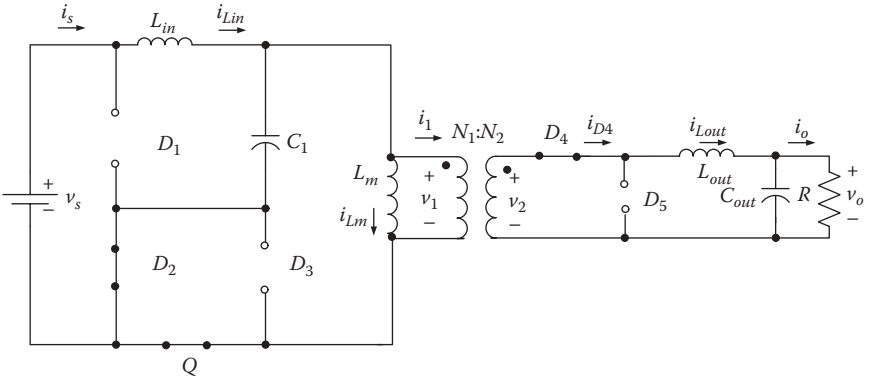


Figure 10.13 Buck integrated forward converter (during DT, switch: on).

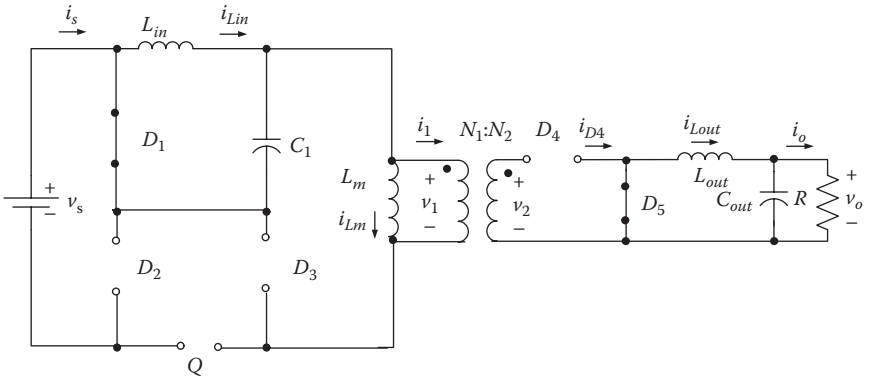


Figure 10.14 Buck integrated forward converter (during Δ_2T, switch: off).

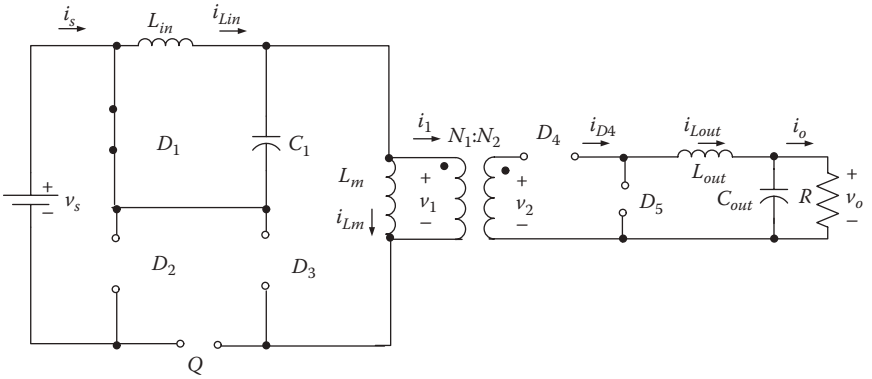


Figure 10.15 Buck integrated forward converter (during (Δ_1– Δ_2) T, switch: off)

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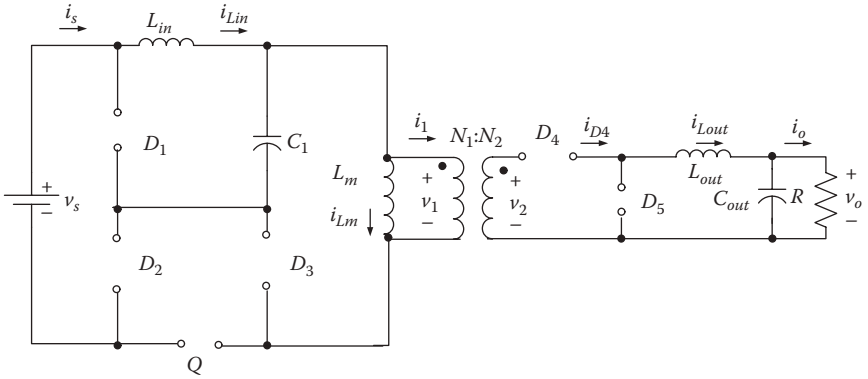


Figure 10.16 Buck integrated forward converter (during (1–D– Δ_1) T, switch: off).

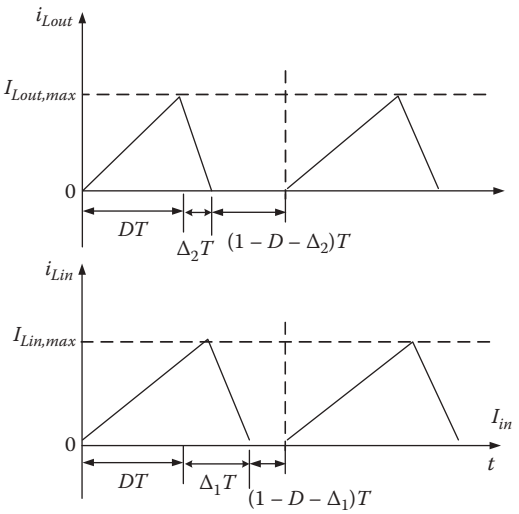


Figure 10.17 Current waveforms for inductors in DCM-DCM ($\Delta_1 > \Delta_2$).

In DCM-DCM ($\Delta_1 < \Delta_2$) mode, both buck converter and forward converter operate in DCM mode for the input inductor L_{in} and output inductor L_{out}. Two kinds of DCM modes are classified by the different time of inductors reaching the zero current after switch is off (Figures 10.18–10.22).

In the next chapter, output/input voltage ratios for the buck integrated forward converter will be discussed.

The voltage ratio for CCM-CCM is shown in Figure 10.23. Voltage ratio for the forward converter in CCM is N_2D/N_1. Voltage ratio for a buck

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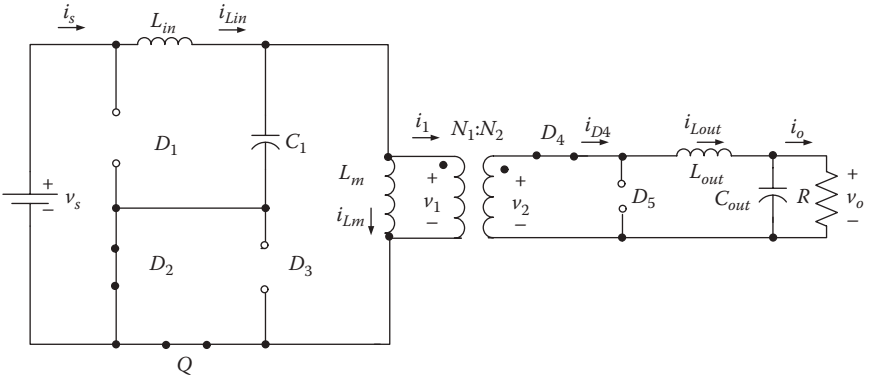


Figure 10.18 Buck integrated forward converter (during DT, switch: on).

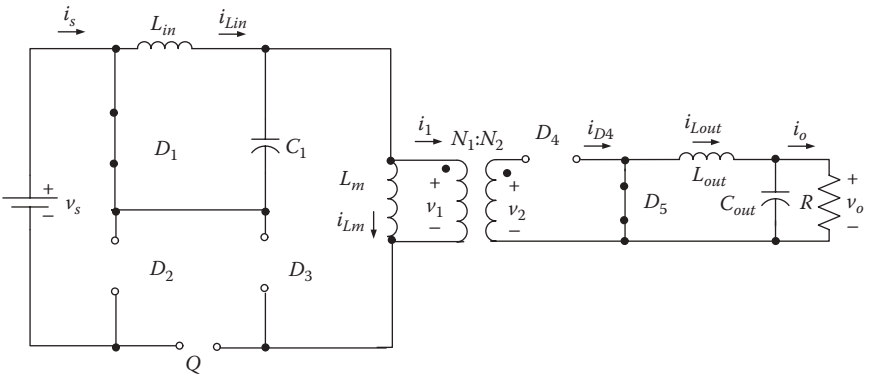


Figure 10.19 Buck integrated forward converter (during Δ_1T, switch: off).

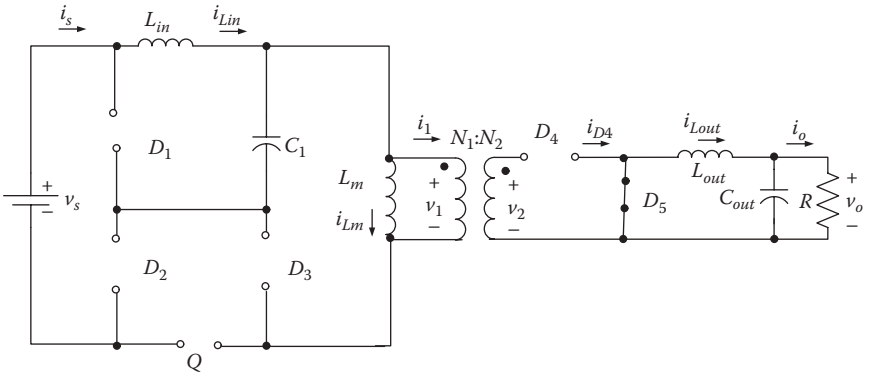


Figure 10.20 Buck integrated forward converter (during (Δ_2 – Δ_1) T, switch: off).

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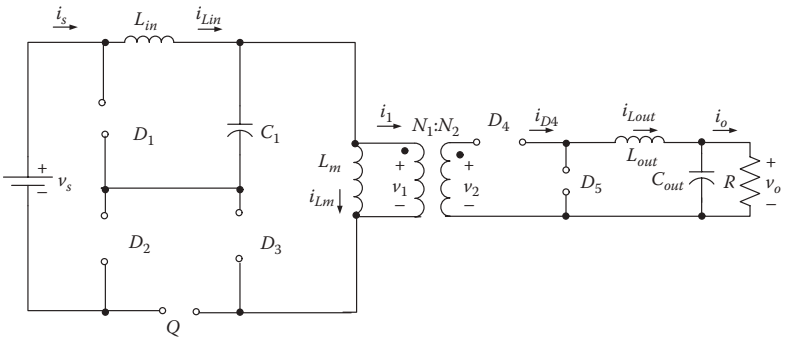


Figure 10.21 Buck integrated forward converter (during (1–D– Δ_2) T, switch: off).

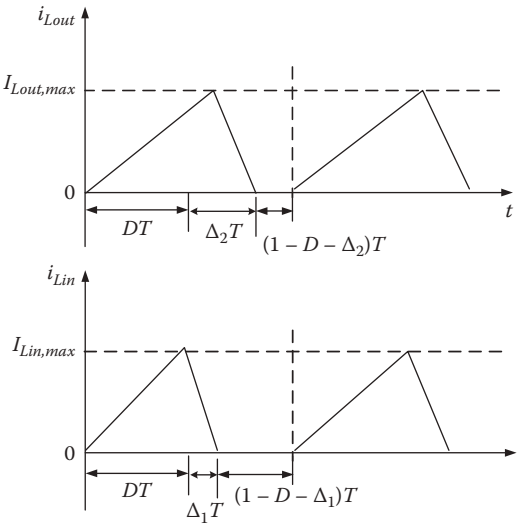


Figure 10.22 Current waveforms for inductors in DCM-DCM ($\Delta_2 > \Delta_1$).

converter in CCM is D. So the overall voltage ratio is $N_2 D^2 / N_1$. In order to reset the forward converter in every cycle, the maximum duty ratio for the buck integrated forward converter is 0.5. According to Figure 10.23, we can see that when the turn ratio for the forward converter transformer is 2, the voltage ratio for the buck integrated forward converter is not greater than that for the buck converter:

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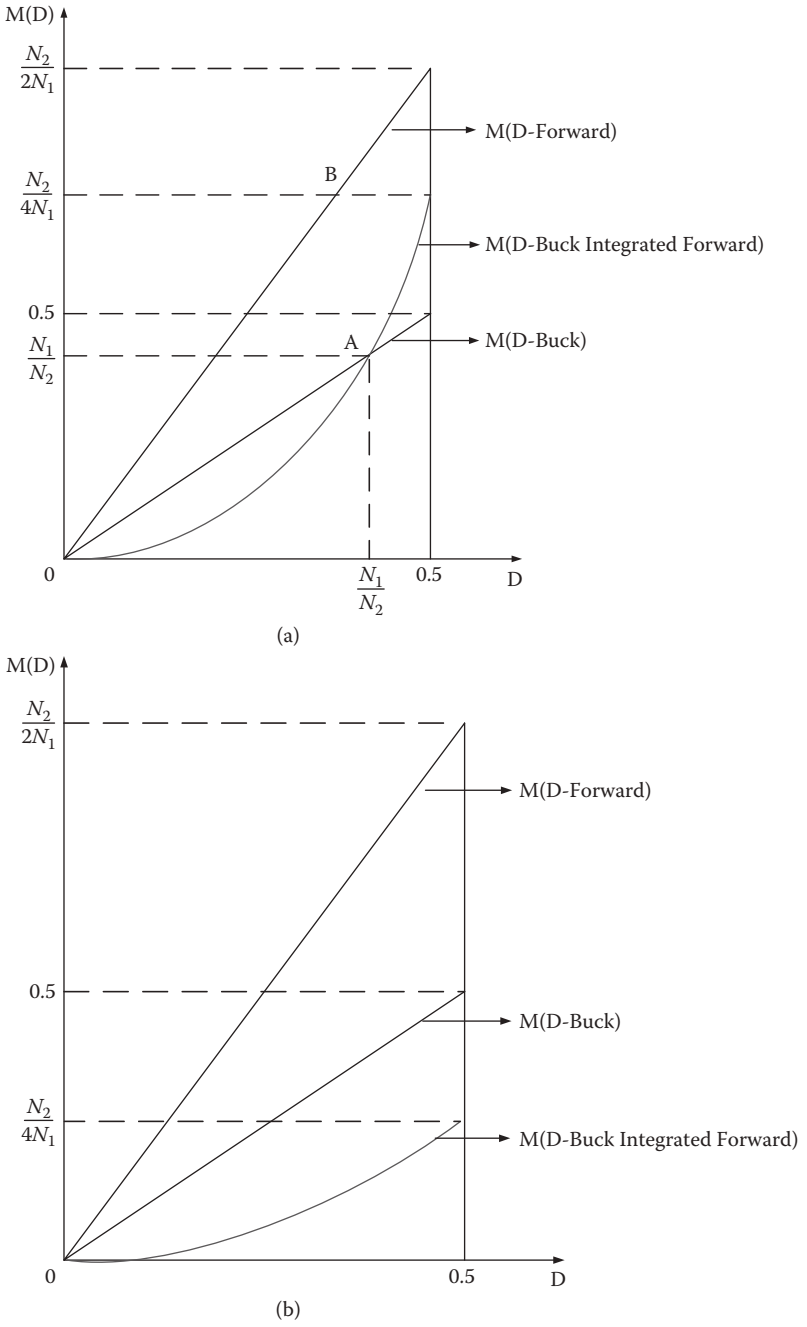


Figure 10.23 Voltage ratio for buck integrated forward converter in CCM-CCM mode.

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$$\left(\frac{N_2}{N_1}D^2 \text{ " } D\right)$$

In this situation, the overall voltage ratio curve is under the buck voltage ratio curve. When the turn ratio for the forward converter transformer is great than 2, the overall voltage ratio is less than that of the forward converter. When $2N_1 \text{ " } N_2$, the output/input voltage ratio is as shown in Figure 10.23(a). When $N_1 \text{ " } N_2 \text{ " } 2N_1$, the output/input voltage ratio is as shown in Figure 10.23(b).

For the buck integrated forward converter in CCM-DCM, the voltage ratios are as shown in Figures 10.24 and 10.25 and

$$k = \frac{2L_{out}}{RT}$$

T is the switch period. For the forward converter operating in DCM, $k \text{ " } (1- D)$ and $k \in 0,1$. Therefore,

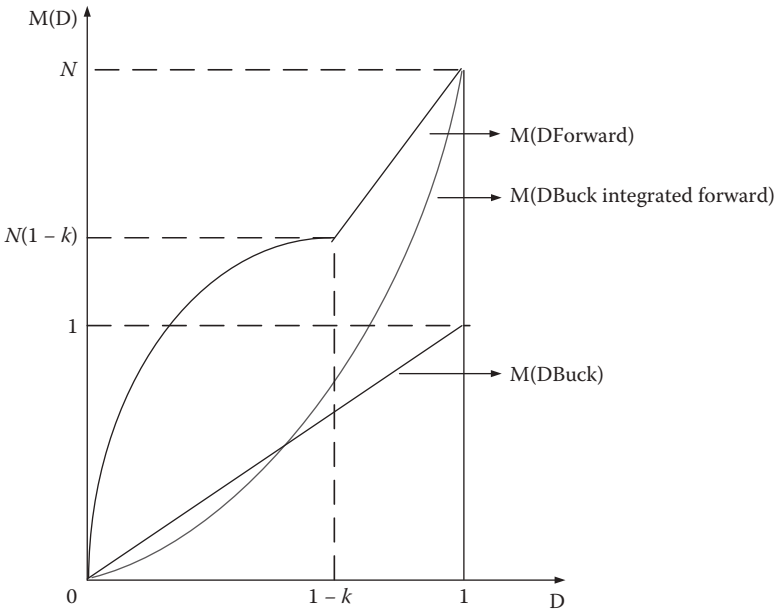


Figure 10.24 Voltage ratio 1 for buck integrated forward converter in CCM-DCM mode.

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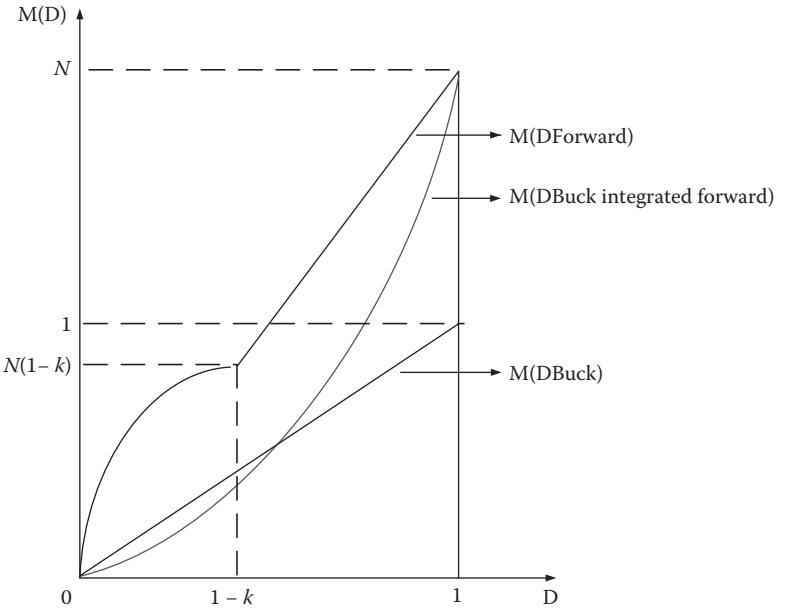


Figure 10.25 Voltage ratio 2 for buck integrated forward converter in CCM-DCM mode.

$$\frac{N_2}{N_1} D'' \quad M(D_{Forward}) = \frac{2N_2 D}{N_1 \quad D + \sqrt{D^2 + \frac{8L_{out}}{RT}}} = \frac{2N_2}{N_1 \quad 1 + \sqrt{1 + \frac{4k}{D^2}}} \quad '' \quad \frac{N_2}{N_1} \tag{10.50}$$

When

$$\frac{N_2(1-k)}{N_1} \geq 1$$

we can find the voltage ratio for the buck integrated forward converter as shown in Figure 10.24.

When

$$\frac{N_2(1-k)}{N_1} < 1$$

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the voltage ratio for the buck integrated forward converter is as shown in Figure 10.25.

Care must be taken to take only the output/input voltage ratio curve where $0 < D'' 0.5$ in Figures 10.24–10.27.

In order to get small signal model for different modes, the buck integrated forward converter with third winding is as shown in Figure 10.28.

In the following paragraphs, CCM-CCM will be analyzed first.

When the switch is on ($0 < t'' dT$), the following formulations can be derived:

$$L_{in}\frac{di_{Lin}}{dt} = V_s - V_{c1} \tag{10.51}$$

$$C_1\frac{dV_{c1}}{dt} = i_{Lin} - i_f \tag{10.52}$$

$$L_{out}\frac{di_{Lout}}{dt} = \frac{N_2}{N_1}V_{c1} - V_o \tag{10.53}$$

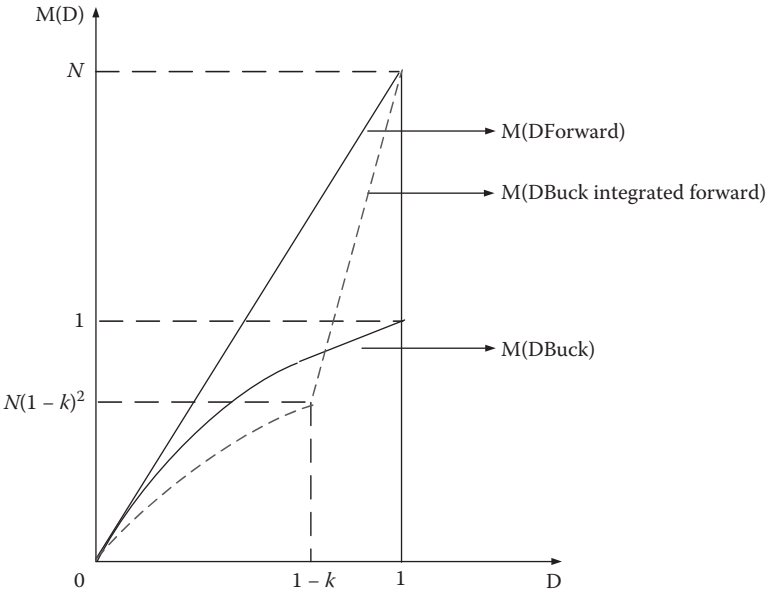


Figure 10.26 Voltage ratio for buck integrated forward converter in DCM-CCM mode

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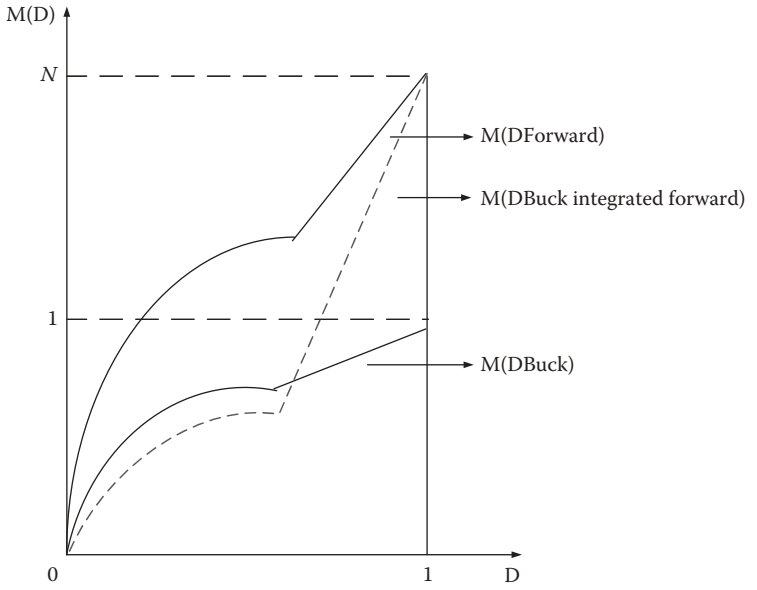


Figure 10.27 Voltage ratio for buck integrated forward converter in DCM-DCM mode.

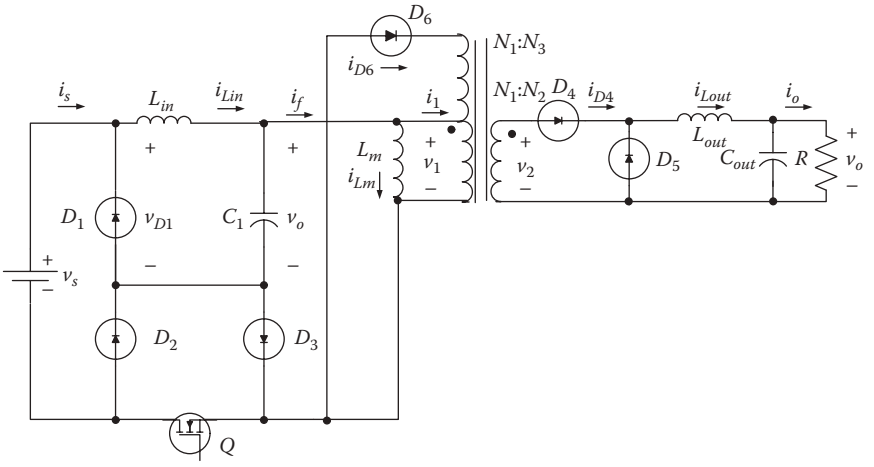


Figure 10.28 Buck integrated forward converter with third winding.

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$$C_{out}\frac{dV_o}{dt} = i_{Lout} - \frac{V_o}{R} \tag{10.54}$$

$$L_m\frac{di_{Lm}}{dt} = V_{c1} \tag{10.55}$$

$$i_f = \frac{N_2}{N_1}i_{Lout} + i_{Lm} \tag{10.56}$$

$$i_s = i_{Lin} \tag{10.57}$$

$$n = \frac{N_2}{N_1} \tag{10.58}$$

When the switch is off, in the period of ($dT < t £ (d + D)T$), $D\,T$ is the time for the transformer to magnetize inductor current from peak to zero. The following formulations are derived:

$$L_{in}\frac{di_{Lin}}{dt} = -V_{c1} \tag{10.59}$$

$$C_1\frac{dV_{c1}}{dt} = i_{Lin} - i_f \tag{10.60}$$

$$L_{out}\frac{di_{Lout}}{dt} = -V_o \tag{10.61}$$

$$C_{out}\frac{dV_o}{dt} = i_{Lout} - \frac{V_o}{R} \tag{10.62}$$

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$$L_m \frac{di_{Lm}}{dt} = -\frac{N_1}{N_3} V_{c1} \tag{10.63}$$

$$i_f = -\frac{N_1}{N_3} i_m \tag{10.64}$$

$$i_s = 0 \tag{10.65}$$

When the switch is off, in the period of ($(d+D)T < t \leq T$), the following formulations are derived:

$$L_{in} \frac{di_{Lin}}{dt} = -V_{c1} \tag{10.66}$$

$$C_1 \frac{dV_{c1}}{dt} = i_{Lin} \tag{10.67}$$

$$L_{out} \frac{di_{Lout}}{dt} = -V_o \tag{10.68}$$

$$C_{out} \frac{dV_o}{dt} = i_{Lout} - \frac{V_o}{R} \tag{10.69}$$

$$L_m \frac{di_{Lm}}{dt} = 0 \tag{10.70}$$

$$i_s = 0 \tag{10.71}$$

Based on the above equations, the average model formulations for the circuit are shown below:

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$$L_{in}\frac{d\langle i_{Lin}\rangle}{dt}=\langle d\rangle\langle V_s\rangle-\langle V_{c1}\rangle \tag{10.72}$$

$$C_1\frac{d\langle V_{c1}\rangle}{dt}=\langle i_{Lin}\rangle-\langle d\rangle\left\langle\frac{N_2}{N_1}i_{Lout}\right\rangle \tag{10.73}$$

$$L_{out}\frac{d\langle i_{Lout}\rangle}{dt}=\langle d\rangle\left\langle\frac{N_2}{N_1}V_{c1}\right\rangle-\langle V_o\rangle \tag{10.74}$$

$$C_{out}\frac{d\langle V_o\rangle}{dt}=\langle i_{Lout}\rangle-\frac{\langle V_o\rangle}{R} \tag{10.75}$$

$$\langle i_s\rangle=\langle d\rangle\langle i_{Lin}\rangle \tag{10.76}$$

In order to get the small signal for the circuit, we need to replace the average variable with steady-state value and small perturbation variables:

$$\langle V_s\rangle=V_s+\hat{V}_s \tag{10.77}$$

$$\langle V_{c1}\rangle=V_{c1}+\hat{V}_{c1} \tag{10.78}$$

$$\langle V_o\rangle=V_o+\hat{V}_o \tag{10.79}$$

$$\langle i_{Lin}\rangle=I_{Lin}+\hat{i}_{Lin} \tag{10.80}$$

$$\langle i_{Lout}\rangle=I_{Lout}+\hat{i}_{Lout} \tag{10.81}$$

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$$\langle d \rangle = D + \hat{d} \tag{10.82}$$

Thus, the small signal equations for the buck integrated forward converter are as follows:

$$L_{in} \frac{d\hat{i}_{Lin}}{dt} = D\hat{V}_s + V_s\hat{d} - \hat{V}_{c1} \tag{10.83}$$

$$C_1 \frac{d\hat{V}_{c1}}{dt} = \hat{i}_{Lin} - \frac{N_2}{N_1} D\hat{i}_{Lout} - \frac{N_2}{N_1} I_{Lout}\hat{d} \tag{10.84}$$

$$L_{out} \frac{d\hat{i}_{Lout}}{dt} = \frac{N_2}{N_1} D\hat{V}_{c1} + \frac{N_2}{N_1} V_{c1}\hat{d} - \hat{V}_o \tag{10.85}$$

$$C_{out} \frac{d\hat{V}_o}{dt} = \hat{i}_{Lout} - \frac{\hat{V}_o}{R} \tag{10.86}$$

$$\hat{i}_s = D\hat{i}_{Lin} + I_{lin}\hat{d} \tag{10.87}$$

Based on these small signal equations, we can calculate the small signal transformer model as shown in Figure 10.29.

When the buck converter operates in DCM and the forward converter operates in CCM, the small signal model for the circuit can be derived as follows:

$$\langle V_s \rangle = \langle V_s \rangle \tag{10.88}$$

$$\langle V_{D1} \rangle = \langle V_{c1} \rangle \tag{10.89}$$

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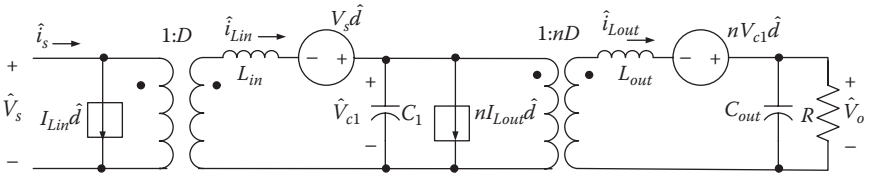


Figure 10.29 Small signal model for buck integrated forward converter in CCM-CCM mode.

$$\langle i_s \rangle = \frac{d^2 T}{2 L_{in}} \langle\langle V_s \rangle - \langle V_{D1} \rangle\rangle = \frac{d^2 T}{2 L_{in}} \langle\langle V_s \rangle - \langle V_{c1} \rangle\rangle \tag{10.90}$$

$$\langle i_{Lin} \rangle = \frac{d^2 T}{2 Lin} \frac{\left(\langle V_s \rangle - \langle V_{c1} \rangle\right)\left(\langle V_s \rangle\right)}{\left(V_{c1}\right)} \tag{10.91}$$

$$C_1 \frac{d\langle V_{c1} \rangle}{dt} = \langle i_{Lin} \rangle - \langle d \rangle \left\langle \frac{N_2}{N_1} i_{Lout} \right\rangle \tag{10.92}$$

$$L_{out} \frac{d\langle i_{Lout} \rangle}{dt} = \langle d \rangle \left\langle \frac{N_2}{N_1} V_{c1} \right\rangle - \langle V_o \rangle \tag{10.93}$$

$$C_{out} \frac{d\langle V_o \rangle}{dt} = \langle i_{Lout} \rangle - \frac{\langle V_o \rangle}{R} \tag{10.94}$$

In order to get the small signal for the circuit, we need to replace the average variable with steady-state value and small perturbation variables:

$$\langle V_s \rangle = V_s + \hat{V}_s \tag{10.95}$$

$$\langle V_{c1} \rangle = V_{c1} + \hat{V}_{c1} \tag{10.96}$$

$$\langle V_o \rangle = V_o + \hat{V}_o \tag{10.97}$$

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$$\langle i_{Lin} \rangle = I_{Lin} + \hat{i}_{Lin} \tag{10.98}$$

$$\langle i_{Lout} \rangle = I_{Lout} + \hat{i}_{Lout} \tag{10.99}$$

$$\langle d \rangle = D + \hat{d} \tag{10.100}$$

Thus, the small signal equations for the buck integrated forward converter are as follows:

$$\hat{i}_s = \frac{D^2 T}{2 L_{in}}\left(\hat{V}_s - \hat{V}_{c1}\right) + \frac{DT}{L_{in}}\left(V_s - V_{c1}\right)\hat{d} \tag{10. 101}$$

$$\hat{i}_{Lin} = \frac{D^2 T\left(2V_s - V_{c1}\right)}{2 L_{in} V_{c1}}\hat{V}_s - \frac{D^2 T V_s^2}{2 L_{in} V_{c1}^2}\hat{V}_{c1} + \frac{DT\left(V_s - V_{c1}\right)V_s}{V_{c1}}\hat{d} \tag{10.102}$$

$$C_1 \frac{d\hat{V}_{c1}}{dt} = \hat{i}_{Lin} - \frac{N_2}{N_1} D\hat{i}_{Lout} - \frac{N_2}{N_1} I_{Lout}\hat{d} \tag{10.103}$$

$$L_{out} \frac{d\hat{i}_{Lout}}{dt} = \frac{N_2}{N_1} D\hat{V}_{c1} + \frac{N_2}{N_1} V_{c1}\hat{d} - \hat{V}_o \tag{10.104}$$

$$C_{out} \frac{d\hat{V}_o}{dt} = \hat{i}_{Lout} - \frac{\hat{V}_o}{R} \tag{10.105}$$

Based on these small signal equations, we can calculate the small signal transformer model as shown in Figure 10.30.

In the same way, small signal models for the buck integrated forward converter in CCM-DCM and DCM-DCM are shown Figures 10.31 and 10.32, respectively.

Transfer function for different modes is analyzed in the following text. Taking the buck integrated forward converter in CCM-CCM as an example, we will derive the control to output and line to output transfer functions based on Figure 10.29.

In order to get the line to output transfer function, we need to set $\hat{d} = 0$ in Figure 10.29. The circuit is as shown in Figure 10.33.

Based on Figure 10.33, we can get the line to output voltage transfer function for the buck integrated forward converter in CCM-CCM:

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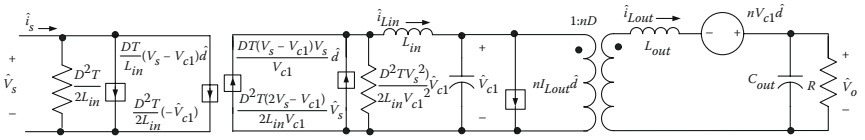


Figure 10.30 Small signal model for buck integrated forward converter in DCM-CCM mode.

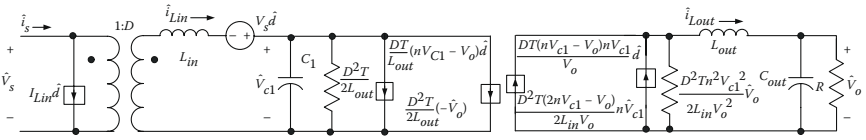


Figure 10.31 Small signal model for buck integrated forward converter in CCM-DCM mode.

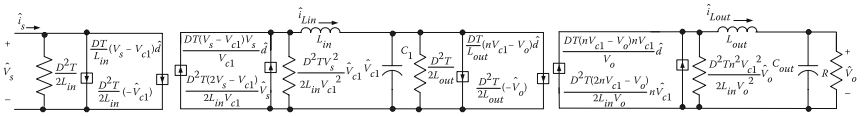


Figure 10.32 Small signal model for buck integrated forward converter in DCM-DCM mode.

$$\frac{\hat{V}_o}{\hat{V}_s} = \frac{nD^2R}{S^4L_{in}L_{out}C_{out}C_1R + S^3L_{in}L_{out}C_1 + S^2\left(n^2D^2RL_{in}C_{out} + L_{in}C_1R + L_{out}C_{out}R\right) + S\left(n^2D^2L_{in} + L_{out}\right) + R} \tag{10.106}$$

In order to determine the duty to output transfer function, we set $\hat{V}_s = 0$ in Figure 10.29, and get Figure 10.34.

Based on Figure 10.31, we can find the line to output voltage transfer function for buck integrated forward converter in CCM-CCM:

$$\frac{\hat{V}_o}{\hat{d}} = \frac{\left(nDV_s + nV_{c1} - n^2DI_{out}SL_{in}\right)R}{S^4L_{in}L_{out}C_{out}C_1R + S^3L_{in}L_{out}C_1 + S^2\left(n^2D^2RL_{in}C_{out} + L_{in}C_1R + L_{out}C_{out}R\right) + S\left(n^2D^2L_{in} + L_{out}\right) + R} \tag{10.107}$$

According to the small signal model and transfer function for the buck integrated forward converter, we can devise the Bode plots shown in Figures 10.35 and 10.36.

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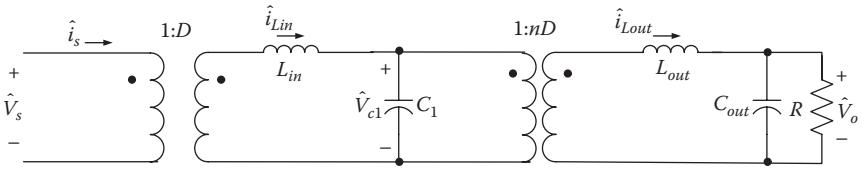


Figure 10.33 Small Signal model with d = 0 for buck integrated forward converter in CCM-CCM mode.

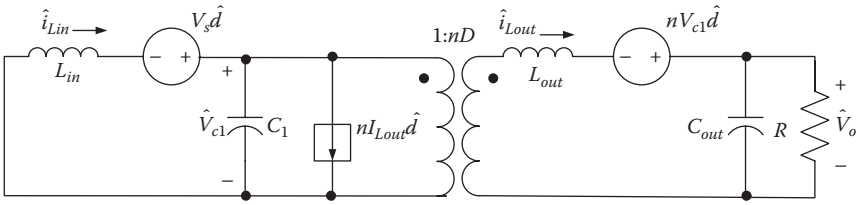


Figure 10.34 Small signal model with $V_s = 0$ for Buck integrated forward converter in CCM-CCM mode.

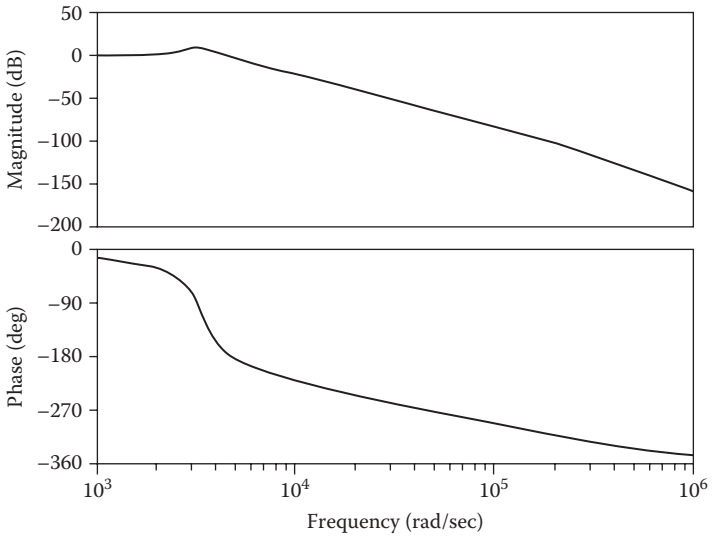


Figure 10.35 Bode plot of line to voltage transfer function for buck integrated forward converter in CCM-CCM mode.

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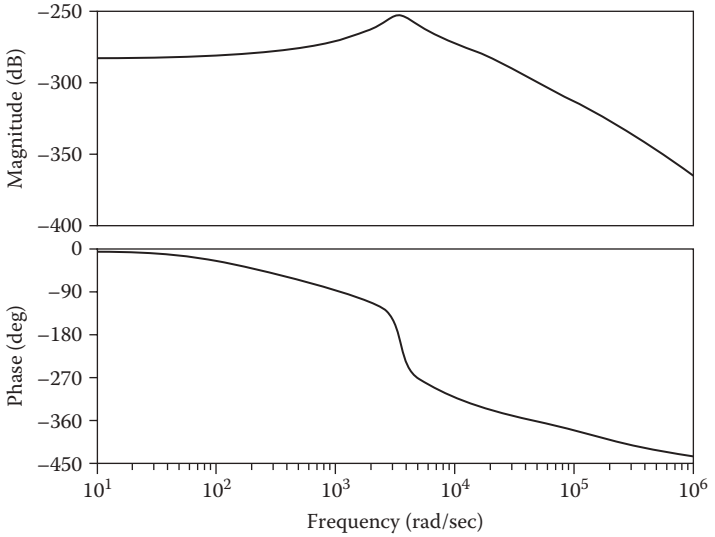


Figure 10.36 Bode plot of duty to voltage transfer function for buck integrated forward converter in CCM-CCM.

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chapter eleven

Synchronous Rectification

Synchronous rectifiers can improve the efficiency of switched-mode power supplies, particularly in low-voltage low-power applications. This chapter compares synchronous rectifiers to Schottky diode types and illustrates some applications.

The next generation of portable products, such as personal communicators and digital assistants, will have to provide at least 12 hours of operation between battery charges. Most of the progress toward this 12-hour goal must come from radio frequency (RF), computer, and battery technology, because power-supply performance is approaching a limit. Typical conversion efficiencies already exceed 95%. Still, the power supply must squeeze a battery for all it is worth. A key element in this task, especially at the low output voltages that future microprocessor and memory chips will need, is the synchronous rectifier.

A synchronous rectifier is an electronic switch that improves power-conversion efficiency by placing a low-resistance conduction path across the diode rectifier in a switched-mode regulator [1]. Metal-oxide–semiconductor field-effect transistors (MOSFETs) usually serve this purpose, but bipolar transistors and other semiconductor switches can be considered for typical applications.

The forward-voltage drop across a switched-mode rectifier is in series with the output voltage, so losses in this rectifier determine efficiency almost entirely [2], [3]. As supply voltage decreases, the design of rectifiers requires more attention, because the forward-voltage drop constitutes an increasing fraction of the output voltage. The race to new voltage levels proceeds in jumps, as each major chip manufacturer brings successive fabrication processes on line. Currently, research indicates a V_{CC} of 1.1 V.

11.1 Selection Criteria for Schottky Diode and MOSFET

The switching regulator's Schottky diode selection is based on its forward-drop and reverse-leakage characteristics. As the output voltage drops, the Schottky diode's forward voltage becomes a limiting factor in improving the converter's efficiency. This limitation forces engineers to use synchronous rectification in applications in which size, efficiency, and thermal

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considerations dominate, such as laptop computers and mobile communications. Even designers of desktop PCs and workstations are turning to synchronous rectification as their power requirements increase and new ICs ease their implementation.

Selection of MOSFET is based on the switching regulator's intended switching speed, efficiency goals, and thermal constraints [4], [5]. These requirements can be translated into MOSFET characteristics such as $R_{DS}(ON)$ and gate charge. As the duty cycle of the main switch increases, $R_{DS}(ON)$ has the most influence on the converter's efficiency. In these types of applications, typically n-channel MOSFETs (NMOS) are used to achieve the lowest possible $R_{DS}(ON)$. For a given die area and breakdown voltage, an NMOS field-effect transistor's (FET's) superior carrier mobility translates to about one half the on-resistance of that of a p-channel device. However, the use of NMOS devices in a high-side configuration complicates the design. An auxiliary supply, a bootstrap circuit, or a charge pump must bring the gate voltage above the source node (input voltage).

11.2 Synchronous Rectification with Basic Switching Power Supply Topologies

Basic topologies for off-line switching power supplies have been discussed in previous chapters. This section deals with application of the synchronous rectification technique to basic switching regulator topologies, for example, buck, boost, and buck-boost [4], [5]. In all of these topologies, the Schottky diode is replaced by MOSFET. The performance of these converters is examined under this operating condition.

11.2.1 Buck Converter with Synchronous Rectification

A standard low-voltage buck regulator uses a MOSFET and a Schottky diode as the two main switching devices (Figure 11.1). Turning the MOSFET on delivers energy to the load and to the inductor. When the MOSFET turns off, the energy in the inductor forces current to circulate

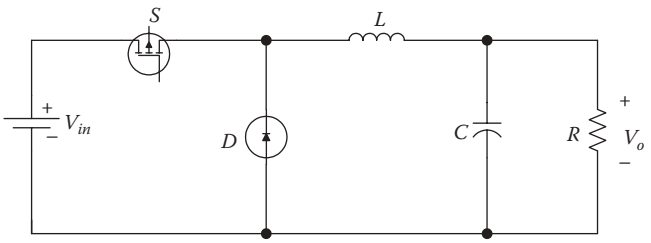


Figure 11.1 Conventional buck converter.

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through the load and Schottky diode. In this manner, the MOSFET switch pulse width modulates the energy.

The inductor and capacitor act as a lowpass filter to restore a nearly constant output voltage. The idealized output voltage is equal to the product of the MOSFET duty cycle and the input voltage.

Synchronous rectification increases the efficiency of a buck converter by replacing the Schottky diode with a low-side NMOS (Figure 11.2). The resultant voltage drop across the MOSFET is smaller than the forward voltage drop of the Schottky diode. A comprehensive comparison includes not only the Schottky diode's forward drop to the third quadrant $R_{DS(ON)}$ of a MOSFET but also the switching losses for both the MOSFET and the Schottky diode. However, at typical operating frequencies and voltages, a buck regulator's switching losses are usually small in comparison to the conduction losses. The low-side MOSFET (for example, synchronous rectifier) conducts current in its third quadrant during the off times of the high-side (main switch) MOSFET. This synchronous switch operates in the third quadrant, because the current flows from the source to the drain, which results in a negative bias across the switch. A positive voltage at the gate of the device still enhances the channel.

The control and driver circuits synchronize the timing of both MOSFETs with the switching frequency. The upper MOSFET (for example, main switch) conducts to transfer energy from the input, and the lower MOSFET (for example, SR in Figure 11.2) conducts to circulate inductor current. The synchronous pulse width modulation (PWM) control block regulates the output voltage by modulating the conduction intervals of the upper and lower MOSFETs. Under light loads, the control block (not shown in Figure 11.2) usually turns the lower MOSFET off to emulate a diode.

Synchronous rectification with discrete MOSFETs causes variable switching delays. This is because of the variations in gate charge and threshold voltage from one MOSFET to another. Standard control circuits compensate for these variations by delaying the turn-on drive of the lower MOSFET until after the gate voltage of the upper MOSFET falls below a threshold. This delay creates a dead time, in which neither MOSFET

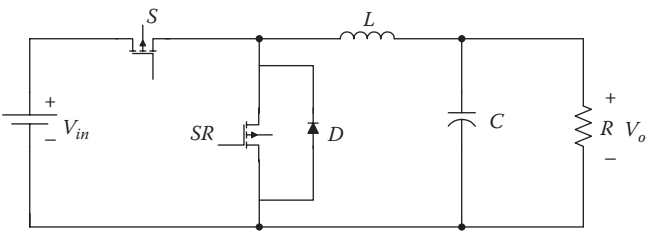


Figure 11.2 Buck converter with synchronous rectifier.

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conducts. The dead time eliminates the possibility of a destructive shoot-through condition; for example, both MOSFETs conduct simultaneously. Standard designs use the same method to delay the turn-on of the main switch. A typical design delays discrete MOSFET conduction with a 60-nsec dead time and limits switching frequency to 300 kHz.

During the dead times, the inductor current flows through the lower MOSFET's body diode and develops stored charge in the depletion region. This stored charge must sweep out to allow the body diode to recover its forward-blocking characteristic. The body diode in a discrete MOSFET has a slow reverse recovery that adversely affects the converter's efficiency. Stored charge can be minimized or eliminated by placing a Schottky diode in parallel with the lower MOSFET. This addition improves the converter's efficiency approximately 1%. The Schottky diode can have a lower current rating than the one that the standard buck regulator uses. This is because the diode conducts only during the dead times, which lowers the RMS current.

Figure 11.3 shows the timing diagram of various parameters of the conventional buck converter circuit. It can be said that the diode conducts for all the time the main switch is off. All this time, the forward voltage drop occurs and that causes significant power loss (Figure 11.4).

The conduction period of the diode, for example, in parallel to SR MOSFET, is very small compared to that of conventional buck converter. This will result in low power loss, and thus improvement in the efficiency.

Even at very low voltages, rectifier loss is significant. For step-down regulators with a 3.3 V output and a 12 V battery input, the 0.4 V forward voltage of a Schottky diode represents a typical efficiency penalty of about 10% to 15%, aside from other loss mechanisms. The losses are not as bad at lower input voltages, because the rectifier has a lower duty cycle and thus a shorter conduction time. However, the Schottky rectifier's forward drop is usually the dominant loss mechanism.

Figure 11.5 shows the efficiency gain using a synchronous rectifier. For an input voltage of 7.2 V and an output of 3.3 V, a synchronous rectifier improves on the Schottky diode rectifier's efficiency by around 4%. This figure also shows that, as output voltage decreases, the synchronous rectifier provides even larger gains in efficiency.

11.2.2 Synchronous Boost Converter

However, it is also possible to incorporate synchronous rectifiers in the boost and inverting topologies. The conventional and synchronous boost regulator and its synchronous counterpart are shown in Figures 11.6 and 11.7.

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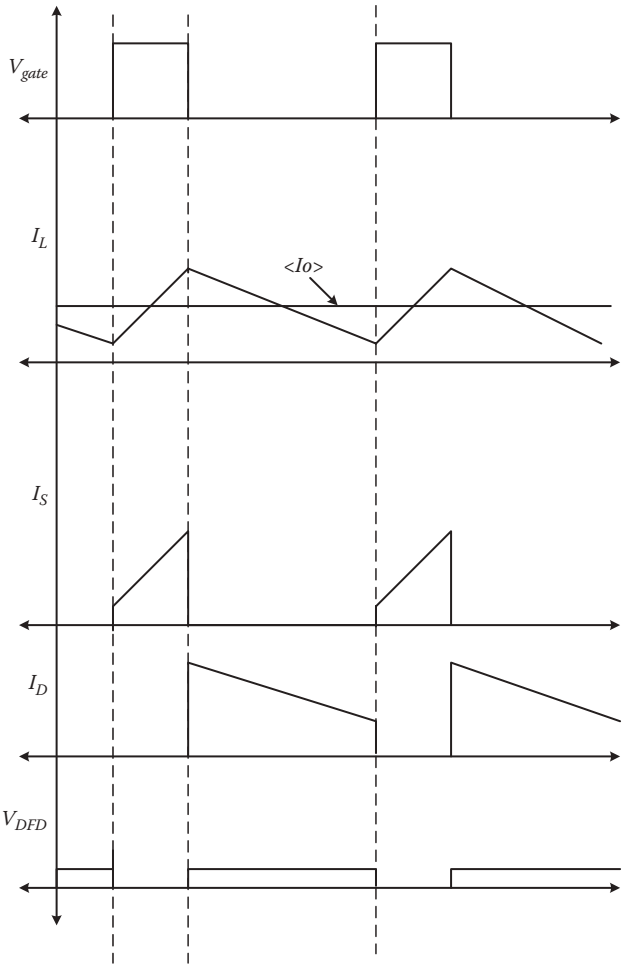


Figure 11.3 Operating mode waveforms of conventional buck converter.

The operation of the synchronous rectified boost circuit is the same as that for the conventional, and the differences are the same as those mentioned for the buck converter in the previous section.

11.2.3 Synchronous Buck-Boost Converter

Inverting topology regulators that generate negative voltages, known as buck-boost regulators, are useful applications for synchronous rectification.

Similar to the boost topology, the inverting topology connects the synchronous rectifier in series with the output rather than to ground. The

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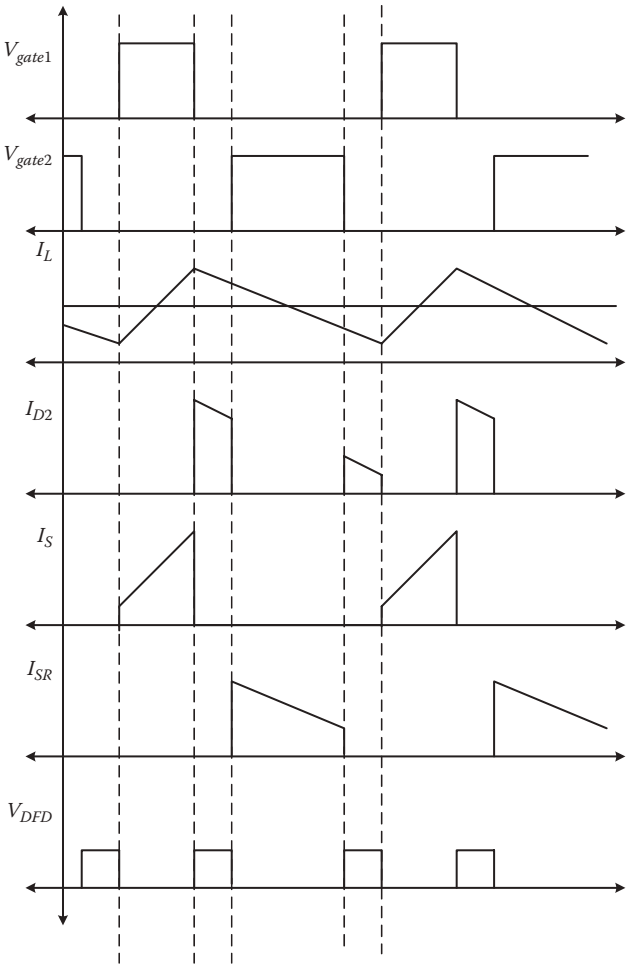


Figure 11.4 Operating mode waveforms of synchronous buck converter.

principle of operation remains the same as that of the conventional buck-boost converter (Figures 11.8 and 11.9).

11.3 Control of Synchronous Rectifier

The synchronous rectified converter uses either current-mode control or voltage-mode control to regulate the output voltage. The current-mode control allows the converter to respond to changes in line voltage without

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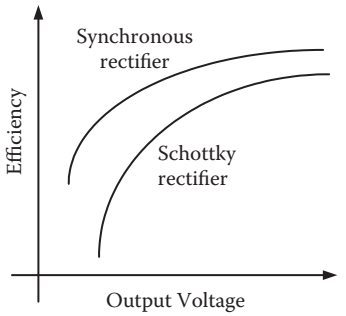


Figure 11.5 Efficiency comparison.

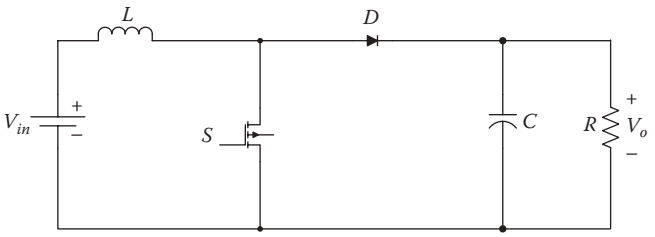


Figure 11.6 Conventional boost converter.

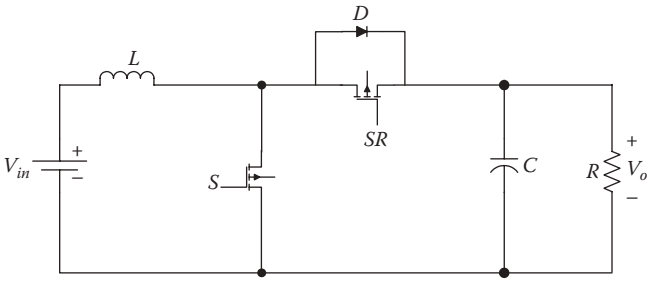


Figure 11.7 Synchronous boost converter.

delay. Also, it is possible to reduce the output inductance to increase the converter's response to dynamic-load conditions.

Although these features would appear to favor current-mode control in applications that require a fast dynamic response, this control method has some disadvantages. For example, it tends to be sensitive to noise in the control loop. Also, the current-mode control method requires two feedback loops: a current inner loop and a voltage outer loop, thus

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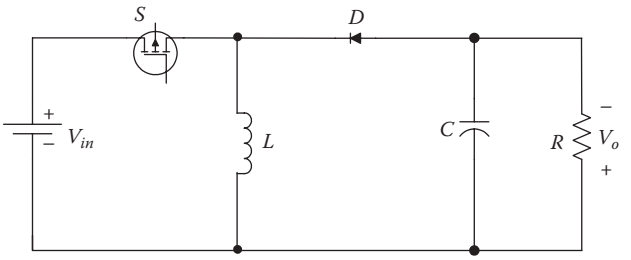


Figure 11.8 Conventional buck-boost converter.

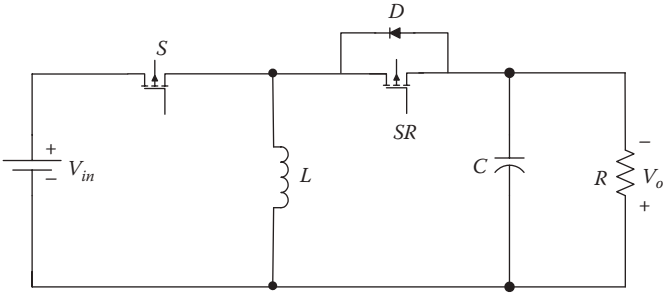


Figure 11.9 Synchronous buck-boost converter.

complicating the design. Finally, the controller uses a current-sensing resistor in series with the output inductor. This current-sensing resistance typically dissipates as much power as do the MOSFETs, further reducing the current-mode converter's efficiency.

Voltage-mode control is attractive for low-voltage buck converters, because it involves a single control loop, exhibits good noise immunity, and allows a wide range for the PWM duty cycle ratio. Also, voltage-mode converters do not require a resistor for sensing current. However, the transfer function of standard voltage-mode buck converters that use Schottky diodes changes from no load to full load, making it difficult to achieve fast response to large dynamic loads.

In the standard buck converter it has been observed that the light-load transfer function exhibits no double pole at the LC filter frequency that is characteristic of the full-load transfer function. This difference occurs because the Schottky diode in the standard buck configuration allows inductor current to flow only in one direction. This unidirectional current flow results in discontinuous operation at light loads in which the inductor runs "dry" during a portion of each cycle, resulting in a single low-frequency pole. The load-current boundary between continuous and

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discontinuous conduction occurs at a load current of one half the peak-to-peak ripple current.

Note that current-mode converters do not exhibit this behavior. The transfer function of a current-mode converter changes only slightly from discontinuous operation to continuous operation. The current-mode controller has two loops. The purpose of the inner, or current, loop is to divide the high-Q double pole of the LC filter into two single, well-separated, low-Q poles. Discontinuous operation exhibits a single low-frequency pole. Due to the popularity of current-mode control over voltage-mode control for synchronous rectifiers, basic current-mode control methods are briefly discussed in next section.

11.4 Current-Mode Control Methods

There are many control ICs available to drive a synchronous rectifier. They implement different control schemes, although there are three basic principles that reside at the heart of any control scheme. First, it is possible to continue to hold the synchronous switch on until the beginning of the next cycle, allowing the inductor to reverse. Second, you can completely disable the synchronous rectifier at light loads. And finally, you can sense the inductor current's zero crossing and shut off the synchronous rectifier on a cycle-by-cycle basis. Each approach involves a trade-off in different areas.

In the past, the option that designers widely used was holding the inductor switch on until the beginning of the next cycle, which requires driving the MOSFET gates with complementary waveforms. This approach produces lower noise and allows a simple control scheme: the gate-drive signal is simply an inverted, opposite-phase version of the drive signal for the high-side switch. Noise is lower for two reasons, both of which relate to the continuous inductor current. First, the absence of pulse skipping ensures a constant switching frequency, regardless of load. A constant, fundamental switching frequency ensures that output ripple and EMI at the harmonic frequencies will not cause havoc in the intermediate frequency (IF) bands of an audio or radio system. Second, this approach eliminates the dead time during which a resonant tank circuit comprising the inductor and stray capacitance at the switching node can introduce ringing.

The drawback of letting the inductor current reverse is that the synchronous rectifier pulls current from the output. The circuit replaces this lost output energy during the next half cycle. However, at the beginning of the cycle when the high-side switch turns on, the circuit transfers the inductor energy stored during the earlier current reversal to the input-bypass capacitor. This action resembles perpetual motion, in which energy shuttles between the input and output capacitors. Unfortunately, friction spoils all perpetual-motion schemes. In this case, the friction consists of

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switching and I^2R losses. As energy shuttles back and forth, the circuit dissipates power in all its tiny parasitic resistances and switching inefficiencies. Thus, additional energy is necessary to maintain the shuttling action. The most obvious consequence is a high no-load supply current of typically 5 mA for the 2.5 V, 1 W circuit.

The second option, turning off the synchronous rectifier entirely at light loads, offers simplicity and low quiescent supply current. You usually implement this method in conjunction with a pulse-skipping operation, governed by a light-load pulse-frequency modulation (PFM) control scheme. Whenever the circuit goes into its light-load pulse-skipping mode, the circuit disables the synchronous rectifier that lets an accompanying parallel Schottky diode do all the work. Disabling the synchronous rectifier prevents the reversal of inductor current, and the problem of shuttling energy back and forth does not arise.

The final option, sensing the inductor current's zero crossing and quickly latching the synchronous rectifier off, turns off the synchronous rectifier on a cycle-by-cycle basis. This method provides the best light-load efficiency, because the synchronous rectifier does its job without allowing the inductor current to reverse. But, to be effective, the switching-regulator IC's current-sense amplifier that monitors the inductor current must combine high speed with low power consumption.

If complementary gate-drive approach is implemented and the output is loaded lightly, the inductor current reverses during the synchronous rectifier's on time and the next half cycle begins with current flowing backward through the high-side MOSFET (MOSFETs are bi-directional). During the switching dead time, current flows through the parasitic diode. A control scheme can shift the synchronous rectifier operation from the complementary-drive option to the off-at-zero option. The control circuit should employ PWM for heavy loads and automatically switch to a low quiescent current pulse-skipping mode for light loads.

Such control comes in handy for computers with built-in radios. When the radio is not in use and the host system goes from run mode to suspend mode, the power supply automatically assumes its light-load pulse-skipping mode to save power. If the RF transceiver is turned on, a logic signal forces the supply to a low-noise mode that maintains quiet operation, regardless of output load.

11.5 *Discrete and Integrated Approach for Synchronous Rectification*

It is possible to have a single IC that integrates the main switch and synchronous rectifier MOSFETs, their drive circuitry, and the synchronous control logic. It is also possible to use such a device along with a simple

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PWM controller to implement voltage-mode converters that have several advantages compared to converters that use discrete MOSFETs. These advantages include improved efficiency, higher switching frequency, reduced EMI, and simplified thermal design. One advantage of the conventional approach over this integrated approach are the wider choice of discrete MOSFETs with a wide range of available $R_{DS}(ON)$s from which to choose. Also, you can tailor discrete MOSFETs to meet an application's efficiency and output current requirements.

However, in contrast to a converter with discrete MOSFETs, an integrated design takes advantage of matched-silicon parameters. Worst-case analysis is less severe, because parameters such as gate charge and threshold tend to track with process variations and operating conditions. Additionally, the body diodes of the integrated MOSFETs exhibit low stored charge and short reverse-recovery times. Integrated power devices also reduce parasitic inductances from the critical high-speed connections.

These performance improvements let one build a converter that reduces dead time to less than 20 nsec, switches with rise and fall times lower than 10 nsec, and operates at frequencies higher than 1 MHz.

When discrete MOSFETs are used, which vendors fabricate using vertical technologies, the substrate is at drain potential. Thus, conductive cooling requires large printed circuit (PC) traces. Large traces increase PC-board area and parasitics that can increase EMI. In contrast, the substrate and the tab of the integrated package are at ground potential. Therefore, heat can transfer directly from the power switches, through the tab, and then to the ground plane.

Why not integrate all the required silicon for the synchronous regulator into a single IC? This level of integration is achievable but involves trade-offs. An IC that integrates the PWM controller, power switches, and drive and synchronous control has greater die size and pinout. Power IC packages with the required pin count and thermal capabilities are expensive. Instead, the silicon partitioning of integrated MOSFET IC allows implementation that has many different PWM controllers to make the final trade-offs, such as current- versus voltage-mode operation.

11.6 Comparison of Diode and Synchronous Rectifiers

When comparing diode and synchronous rectifiers, note that the synchronous rectifier MOSFET does not always replace the usual Schottky diode.

The gate-drive signal is a key factor in calculating a synchronous rectifier's efficiency gain. For example, it is possible to reduce gate loss by using a gate drive of 5 V (as for logic-level MOSFETs) instead of the input (battery) voltage. One can simply supply the gate drive from a 5 V linear

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regulator powered from the battery. Better yet, bootstrap the gate driver's power-supply rails from the regulator's output voltage. (This approach adds complexity in the form of a bypass switch for the initial power-up.) Also, one must weigh the lower loss associated with reduced gate voltage against the higher $R_{DS(ON)}$ resulting from a less-enhanced MOSFET.

To prevent switching overlap of the main switch and synchronous rectifier MOSFETs that might cause destructive cross-conduction currents, most switching regulators include a dead-time delay. The synchronous rectifier MOSFET contains an integral, parasitic body diode that can act as a clamp and catches the negative inductor voltage swing during this dead time. However, this body diode is lossy, is slow to turn off, and can cause a 1% to 2% efficiency drop.

Therefore, designers interested in squeezing the last percent of efficiency from a power supply generally place a Schottky diode in parallel with the synchronous rectifier MOSFET. This diode conducts only during the dead time. A Schottky diode in parallel with the silicon body diode turns on at a lower voltage, ensuring that the body diode never conducts. Generally, a Schottky diode used in this way can be smaller and cheaper than the type the simple buck circuit requires, because the average diode current is low. (Schottky diodes usually have peak current ratings much greater than their DC current ratings.)

Conduction losses during the dead time can become significant at high switching frequencies. For example, in a 300 kHz converter with a 100 nsec dead time, the extra power dissipated is equal to $I_{LOAD} \times V_{FWD} \times td \times f = 6$ mW (where f is the switching frequency and td is the dead time) for a 2.5 V, 1 W supply, which represents an efficiency loss of about 0.5%.

Light-load efficiency is a key parameter for mobile applications in which the computer spends a long time in a nearly dormant suspend mode. For the buck-type switched-mode regulators often used in portable equipment, the synchronous rectifier's control circuit has a strong influence on light-load efficiency and noise performance. The key issue for light-load or no-load conditions is the timing of the MOSFET's turn-off signal.

When load current is light, the inductor current discharges to zero, becoming discontinuous or reversing direction. Many control strategies have been proposed to deal with this problem. The fundamental principles of controlling the synchronous switch are briefly described in the preceding section.

11.7 Simulation Results

To demonstrate the effectiveness of the synchronous rectification and also to verify the theory presented here, a buck converter for a 3 V, 18 W application is simulated and results are obtained for both a Schottky diode rectifier and a MOSFET synchronous rectifier. From the results shown

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in Figures 11.10–11.13 it can be concluded that synchronous rectification improves the efficiency to a great extent.

Table 11.1 lists the parameters of the simulated buck converter. The parameters are kept exactly the same for the synchronous buck converter. This is necessary to check the efficiency improvement by synchronous rectification.

From the waveform shown in Figure 11.11 the average power loss due to the conduction of the Schottky diode is calculated. This loss is 2.7 W. For an 18 W application, this loss results in efficiency of 85%.

Figure 11.12 shows the inductor current, main switch current, synchronous rectifier current, and current through the diode connected in parallel with the synchronous rectifier. This figure confirms that there is no difference in operation compared with conventional buck converter. On the other hand, the average power loss calculated from Figure 11.13 is 0.27 W. For an 18 W application, this loss results in 98.5% efficiency, which shows around 15% improvement in the efficiency.

The basic trade-off between using diode or MOSFET rectifiers is whether the power needed to drive the MOSFET gate cancels the efficiency gained from a reduced forward-voltage drop. The synchronous rectifier's efficiency gain depends strongly on load current, battery voltage, output voltage, switching frequency, and other application parameters. Higher battery voltage and lighter load current enhance the value of a synchro-

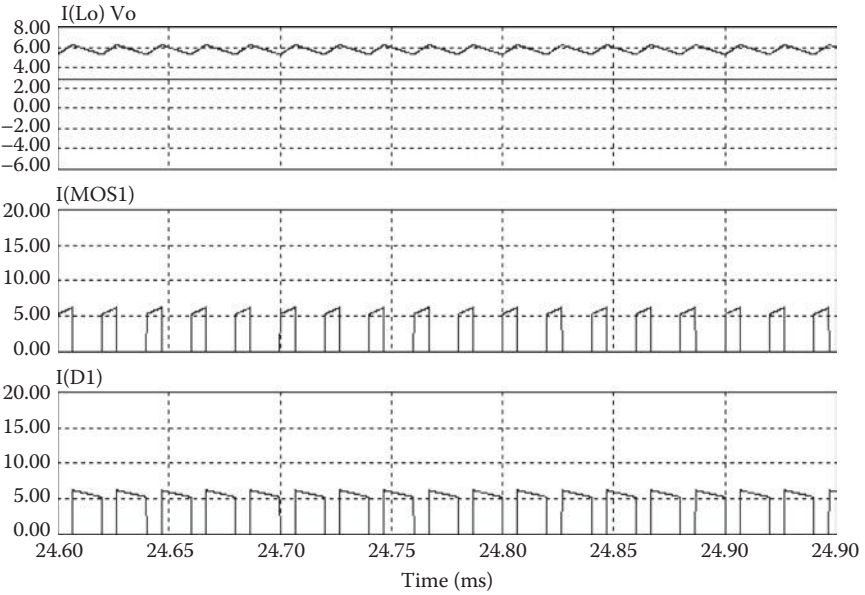


Figure 11.10 Current of D, S and L for conventional buck converter.

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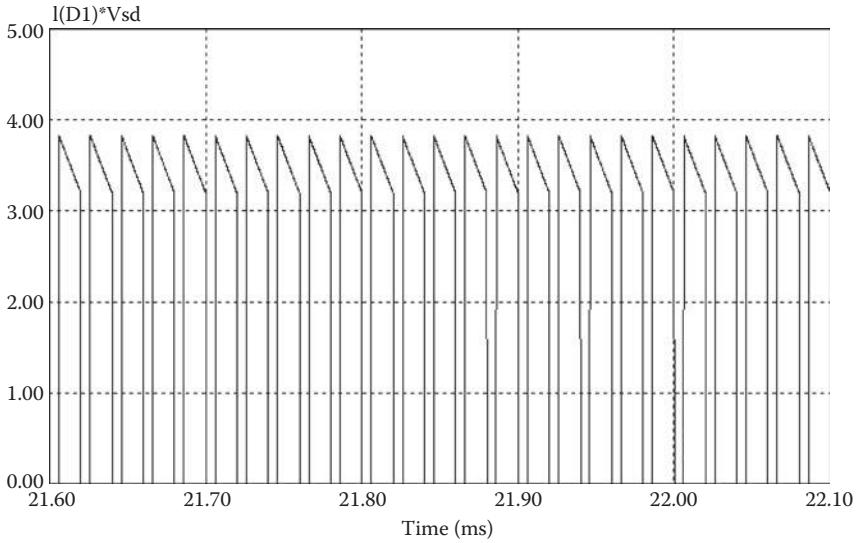


Figure 11.11 Power losses in buck converter Schottky rectifier.

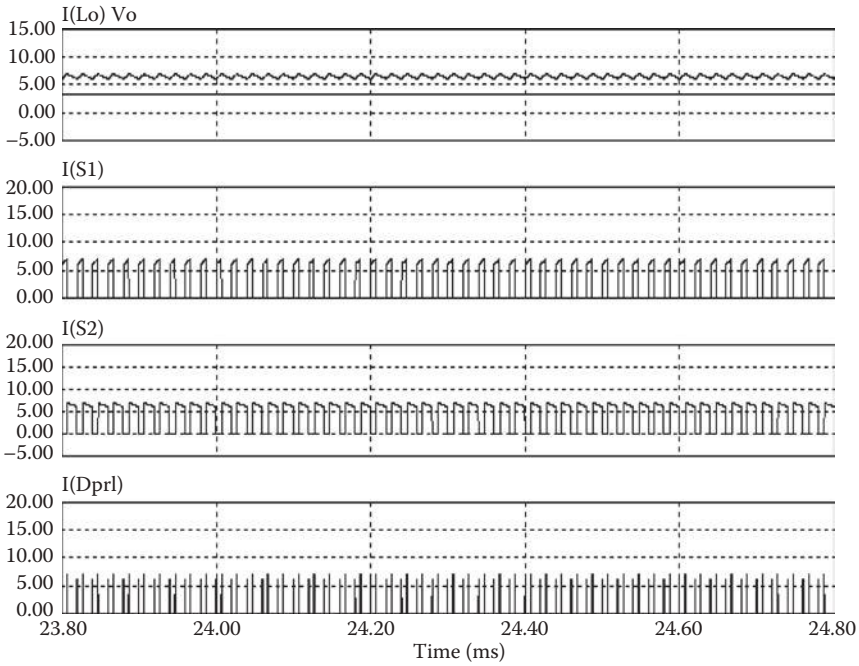


Figure 11.12 Synchronous buck converter component currents.

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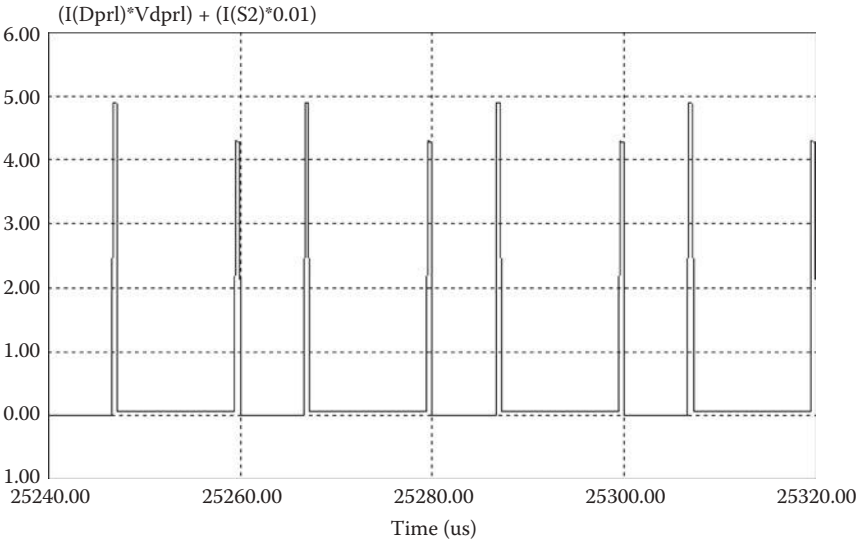


Figure 11.13 Total power loss in synchronous buck converter.

Table 11.1 Parameters of Buck Converter with Schottky Rectifier

Parameter	Value
Input voltage, V_{dc}	10
Switching frequency, f_s	50 k
Output voltage, V_{out}	3
Inductance, L	50 u
Capacitance, C	500 u

nous rectifier. The duty ratio for the main switch increases with the battery voltage. Also, the forward drop decreases with the load current.

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chapter twelve

Synchronous Rectification with Flyback and Forward Converters

The conduction loss of the diode rectifier contributes significantly to the overall power loss in a power supply, especially in low output voltage applications. The rectifier conduction loss is proportional to the product of its forward-voltage drop and the forward conduction current. On the other hand, operating in the MOSFET III quadrant, a synchronous rectifier presents a resistive characteristic, as shown in Figure 12.1. Under a certain current level, the forward voltage drop of a synchronous rectifier can be lower than that of a diode rectifier, and consequently reduces the rectifier conduction loss [1]. Due to the fact that synchronous rectifiers are active devices, the design and utilization of synchronous rectification needs to be properly addressed.

This chapter analyzes the application of synchronous rectification in two of the most popular isolated topologies: flyback and forward converters. Conversion efficiencies of different implementations are compared and verified with simulation results.

12.1 Synchronous Rectification in the Flyback Converter

A number of applications of synchronous rectification in the flyback converter have been reported. However, in all of these applications, the main purpose of the synchronous rectifier (SR) was to provide the post-regulation of the output voltage and not to maximize the conversion efficiency. Specifically, the SR is used as a voltage-controlled resistor in a control loop, which adjusts the converter's resistance so that the output voltage is maintained within the regulation range. Generally, the regulation range of these post-regulation approaches is limited to the forward voltage drop of the SR body diode. Moreover, since the voltage drop across the SR is not minimized because of the resistance modulation, the conversion efficiency of these post-regulators is reduced, compared to that of the converter with the "true" SR.

This section evaluates various implementations of the flyback converter with the SR, with respect to the corresponding converter with the diode rectifier. Specifically, performance evaluations of the constant-

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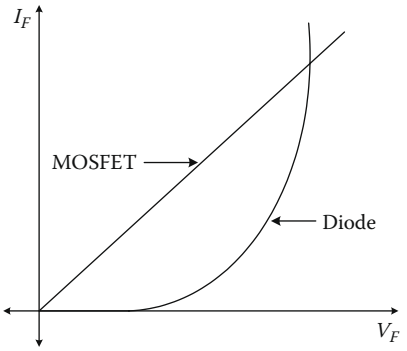


Figure 12.1 MOSFET and Schottky characteristic.

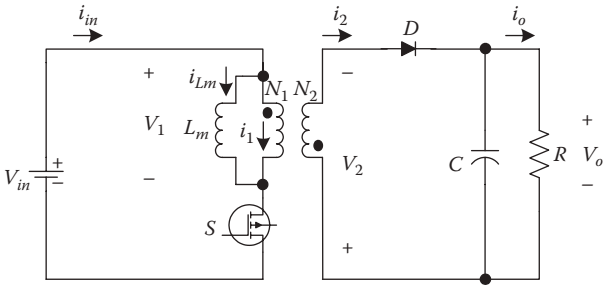


Figure 12.2 Conventional flyback converter.

frequency (CF) continuous-conduction-mode (CCM), CF discontinuous-conduction-mode (DCM), variable-frequency (VF) DCM, and zero-voltage switched (ZVS) DCM flyback converters with SR are discussed. The simulation results have been provided to justify the theoretical claims.

12.1.1 Constant-Frequency Continuous Conduction Mode

A conventional flyback converter and one with the SR are shown in Figures 12.2 and 12.3, respectively [2], [3]. For proper operation of the converter, conduction periods of primary switch (S) and secondary-side switch SR must not overlap for the flyback converter with synchronous rectification. To avoid the simultaneous conduction of the S and the SR, a delay between the turnoff instant of S and the turn-on instant of the SR as well as between the turn-on instant of the S and turn-off instant of the SR must be introduced in the gate drive signals of the switches.

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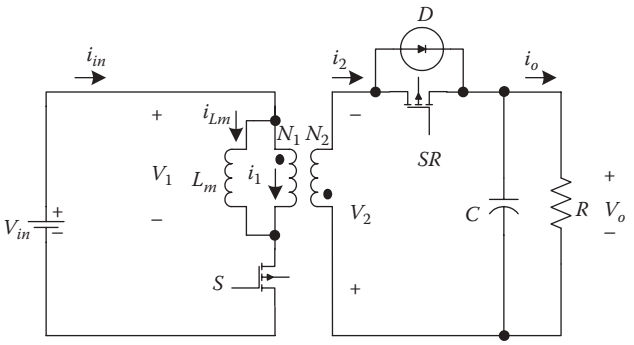


Figure 12.3 Synchronous flyback converter.

With properly designed gate drives, the operation of the circuit shown in Figure 12.3 is identical to that with a conventional diode rectifier (Figure 12.2). Power stages of the flyback converter at different operating instances are shown in Figure 12.4. When the time switch SW is turned on, energy is stored in the transformer magnetizing inductance and is transferred to the output after SW is turned off.

The key waveforms of the conventional flyback converter and one with synchronous rectification, both operating in CCM, are given in Figures 12.5 and 12.6, respectively.

As can be seen from the timing diagrams, during delay times (both on and off), secondary current flows through the body diode of the SR. The conduction of the body diode not only increases the conduction loss, but also introduces a reverse recovery loss when the primary switch S is turned on. The conduction loss of the SR is given by the sum of the channel resistance loss and body diode loss.

In addition to conduction and reverse recovery losses, the CF CCM flyback converter exhibits a loss each time the SR is turned off (for example, each time the SW is turned on) because of a parasitic resonance between synchronous switch capacitance and the leakage inductance of the transformer. The parasitic resonance is damped by a snubber, which also limits the maximum voltage across the SR, and it dies out completely before the SR is turned on again.

Finally, for proper operation of the circuit, the SR must be turned off before the primary SW is turned on. Therefore, the flyback converter with the SR cannot be self-driven from the secondary winding of the transformer. In fact, the circuit shown in Figure 12.3 requires an external control circuit to turn off the SR.

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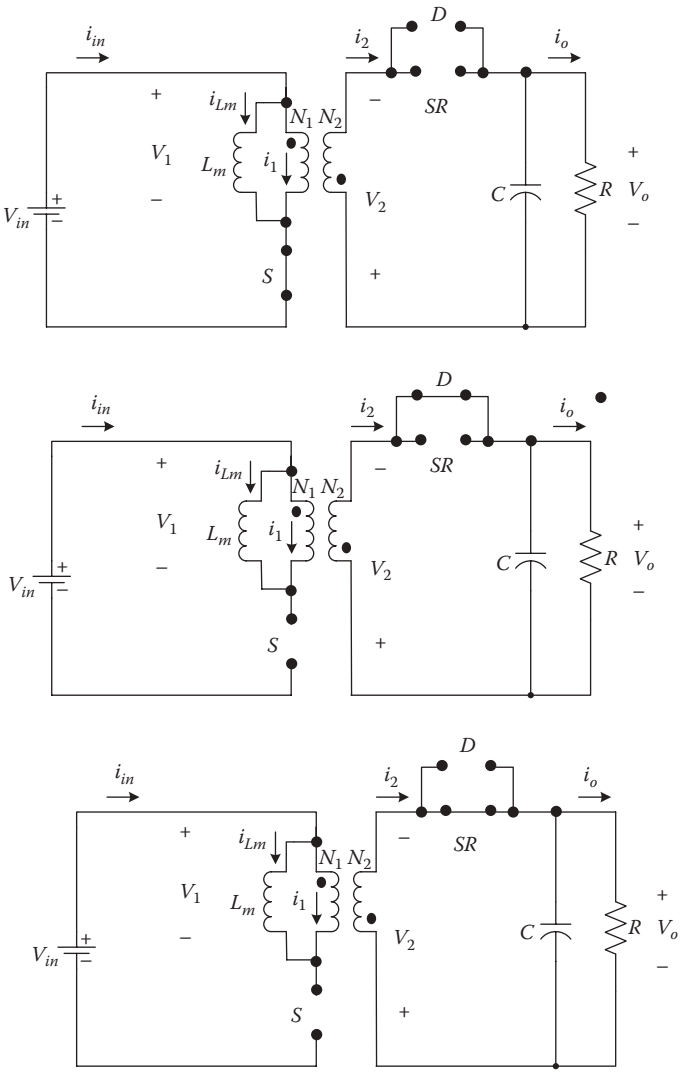


Figure 12.4 Operating stages of synchronous flyback converter.

12.1.2 *Flyback Converter with Constant-Frequency Discontinuous Conduction Mode*

The key waveforms of the constant-frequency, conventional flyback converter and one with the SR operating in DCM are shown in Figure 12.7. In DCM [4], the energy stored in the magnetizing inductance of the transformer during the on time of switch S is completely discharged during the

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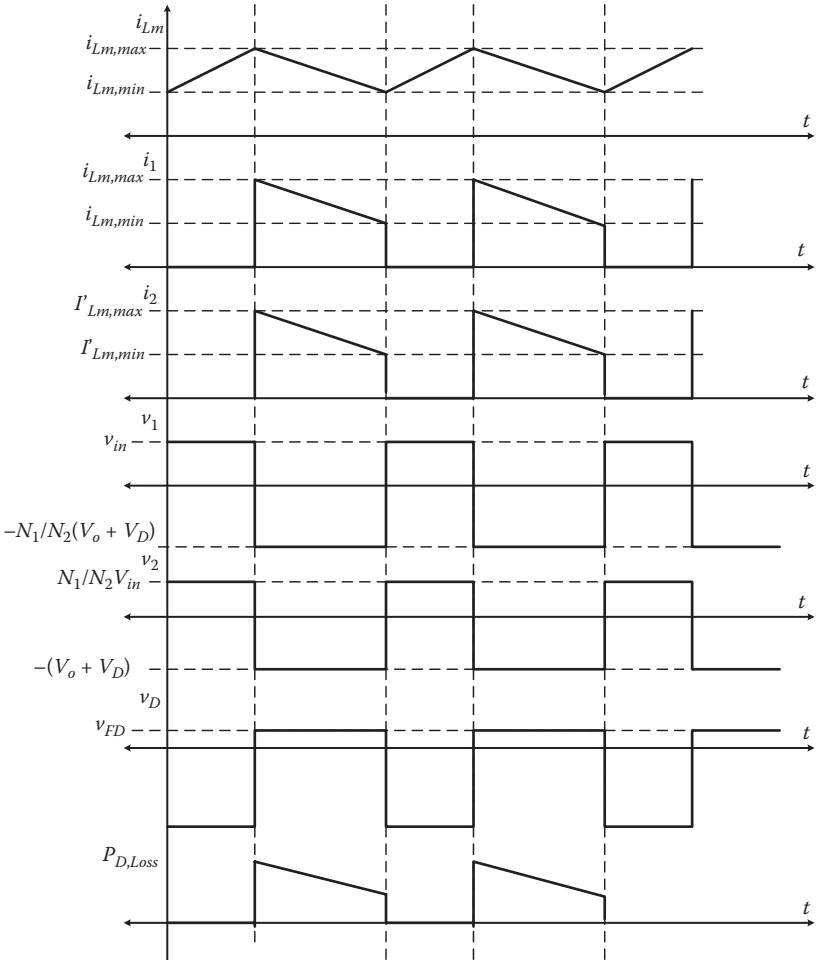


Figure 12.5 Operating waveforms of conventional flyback converter.

subsequent off time. As can be seen from Figure 12.7, secondary current reaches zero before primary switch S is turned on. To prevent the discharging of the output filter capacitor through a conducting SR, the SR channel conduction must be terminated at the moment or soon after the secondary reaches zero.

Therefore, the DCM flyback converter with the SR requires a zero-current crossing detector in the control circuit. After the SR is turned off, the magnetizing inductance of the transformer and equivalent primary side capacitance starts resonating (Figure 12.8).

For a converter with a regulated output, the duration of resonant interval changes significantly with the input voltage and less dramatically

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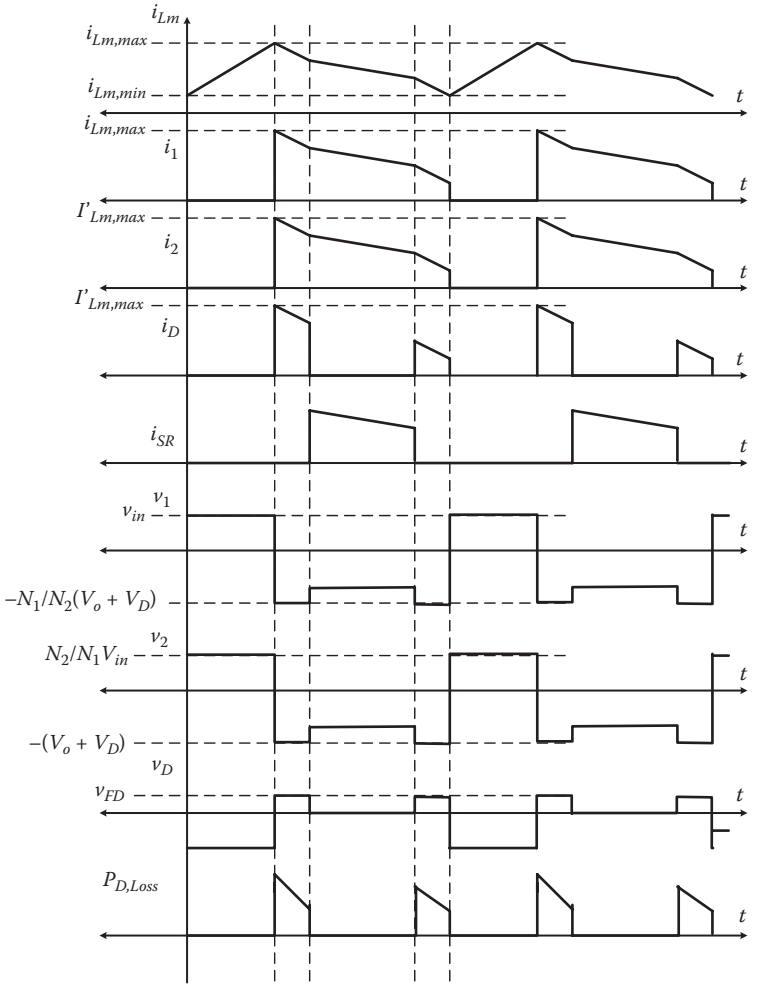


Figure 12.6 Operating waveforms of synchronous flyback converter.

with the output current. As a result, the voltage across the primary switch at the moment of its turn on can range anywhere between $V_{in} + nV_o$ and $V_{in} - nV_o$.

The efficiency of the converter has strong fluctuations with the input voltage. Because typical SRs have a much larger output capacitance than Schottky rectifiers, the characteristic impedance of the resonant tank consisting of magnetizing inductance of transformer and equivalent primary side capacitance, is much lower for a converter with an SR compared to that with a Schottky diode. As a result, the resonant-tank

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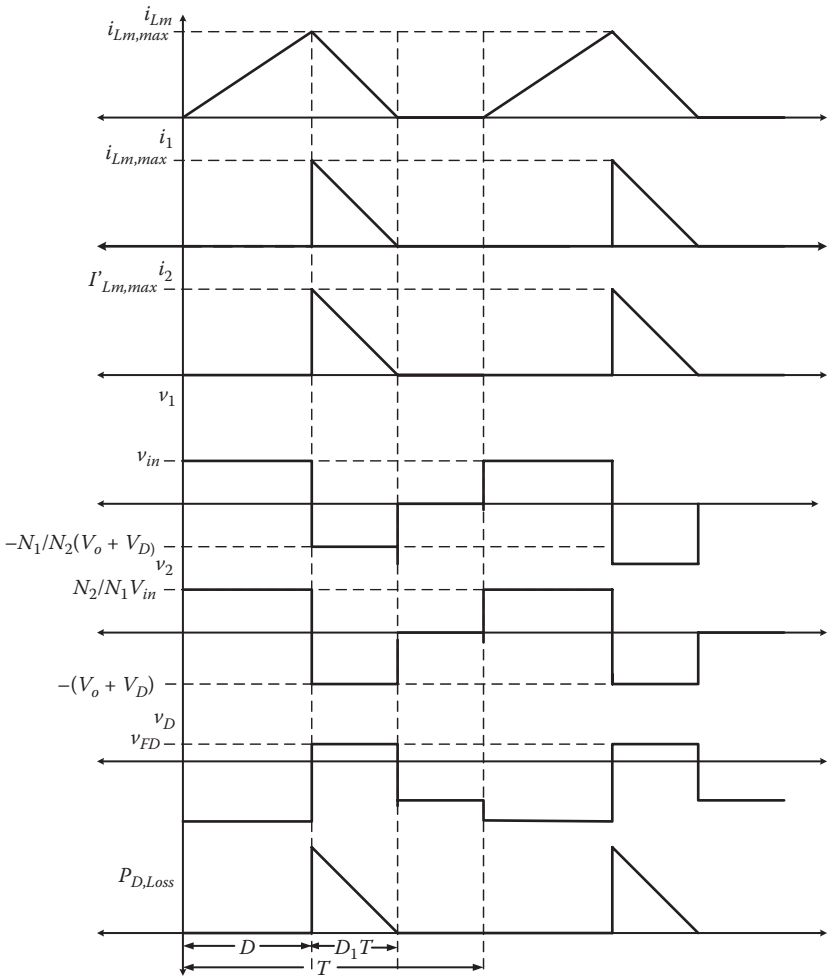


Figure 12.7 Operating waveforms of conventional flyback in DCM.

current of the converter with an SR is much higher than that of the converter with a Schottky, causing a larger conduction loss. For certain line and load conditions, this power loss can completely offset the conduction power loss savings obtained by the SR, making the efficiency of the converter with the SR lower than that of the converter with the diode rectifier (Table 12.1).

Finally, it must be noted that in the DCM flyback converter, reverse rectifier loss PR SR is eliminated because the rectifier current becomes zero before primary switch SW is turned on.

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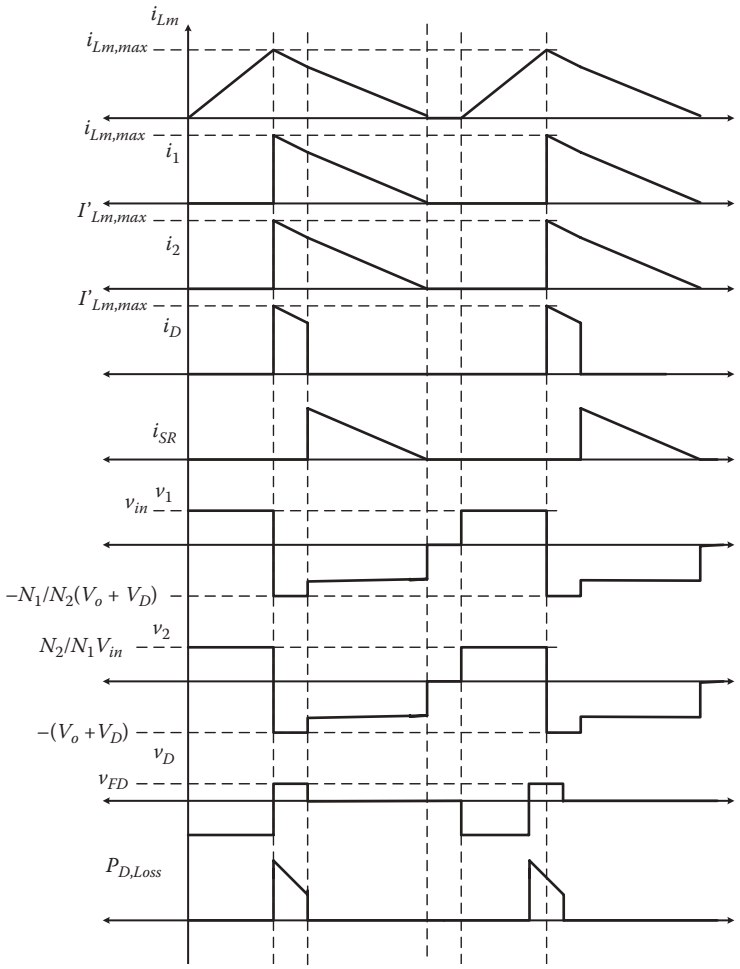


Figure 12.8 Operating waveforms of synchronous flyback in DCM.

Table 12.1 Parameters for Flyback Converter with Schottky Rectifier

Parameter	Value
Input voltage, V_{dc}	9
Switching frequency, f_s	50 k
Output voltage, V_{out}	1.5
Inductance, L_m	20 u
Capacitance, C	600 u
Turns ratio, n	1

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12.1.3 Flyback Converter with Variable-Frequency Discontinuous Conduction Mode

If MOSFET with its parasitic capacitance is considered, as shown in Figure 12.9, then under the variable-frequency DCM operating condition, the waveforms of various parameters can be obtained as shown in Figure 12.10.

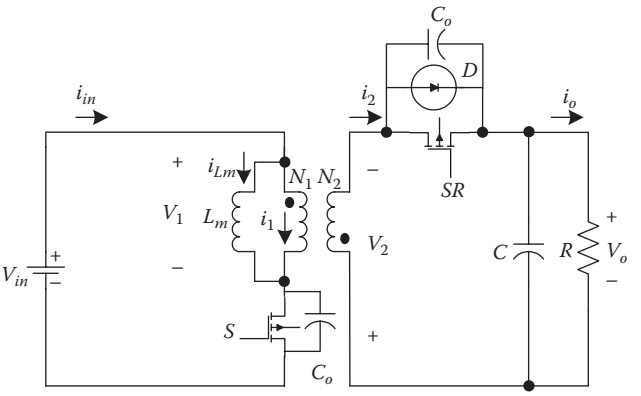


Figure 12.9 Synchronous flyback converter with parasitic capacitance.

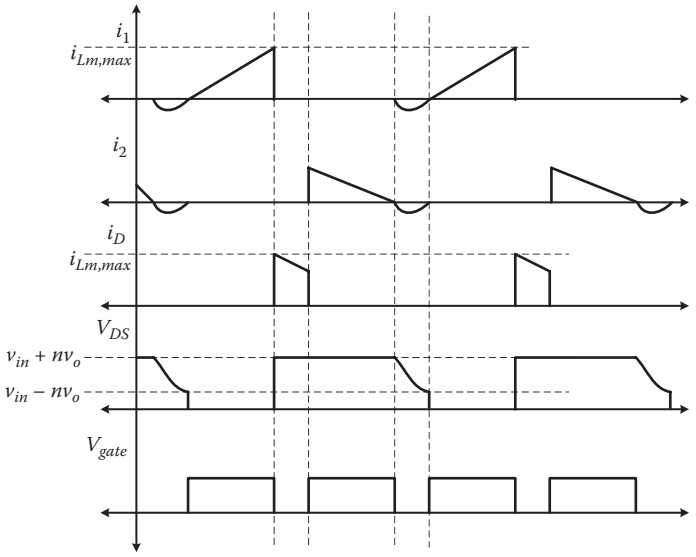


Figure 12.10 Operating waveforms for VF DCM synchronous flyback converter.

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Capacitive switching loss can be minimized, and parasitic oscillation caused by the interaction between the magnetizing inductance of the transformer and equivalent primary capacitance can be eliminated if the primary switch SW is turned on at the moment when the switch voltage reaches its minimum voltage, for example, $V_{in} - nV_o$, the first time after the SR is turned off. This can be accomplished by sensing the zero current crossing of transformer secondary current and turning on the main switch S after a constant delay, which is almost equal to one half of the parasitic resonance period.

With this variable-frequency control, the efficiency fluctuations with the input voltage are eliminated. It should be noted that with the VF control, the switching frequency is minimum at low line and full load, and it increases as the line increases and/or load decreases. The conversion efficiency at low line of the variable-frequency DCM converter can always be made higher than the efficiency of the corresponding constant-frequency counterpart. In addition, the efficiency of the VF DCM converter can also be higher than that of the CF DCM implementation if the power-loss savings due to the elimination of the parasitic oscillations and the minimization of the turn-on voltage are higher than the increased switching losses and magnetic losses due to the increased switching frequency.

12.1.4 Flyback Converter with VF DCM Zero-Voltage Switching

As can be seen from Figure 12.10, if the amplitude of the oscillation after the turn-off of the SR is larger than the input voltage, for example, if $V_{in} < nV_o$, primary-switch voltage VDS will fall to zero before the switch is turned on [5], [6]. Therefore, for $V_{in} < nV_o$, the variable frequency flyback converter can achieve ZVS [7], [8], for example, the capacitive turn-on loss of the primary switch can be eliminated. While the ZVS condition may be met for certain designs at low input voltages, generally it is not met at higher input voltages. As a result, at higher input voltages, the VF flyback converter with gate-drive timing given in Figure 12.10 operates with partial ZVS.

However, the complete ZVS of the primary switch in the VF flyback converter with the SR can be achieved in the entire input-voltage range if the turn-off instant of the SR after the secondary current zero crossing is delayed enough to allow a negative secondary current to build up, as shown in Figure 12.11. To achieve ZVS in the entire input voltage range, the energy stored in magnetizing inductance L_m by the negative secondary current must be large enough to discharge primary switch capacitance, from voltage $V_{in} + nV_o$ down to zero. Therefore, to build up the necessary ZVS current, the turn-off of the SR should be delayed after the zero crossing of secondary current.

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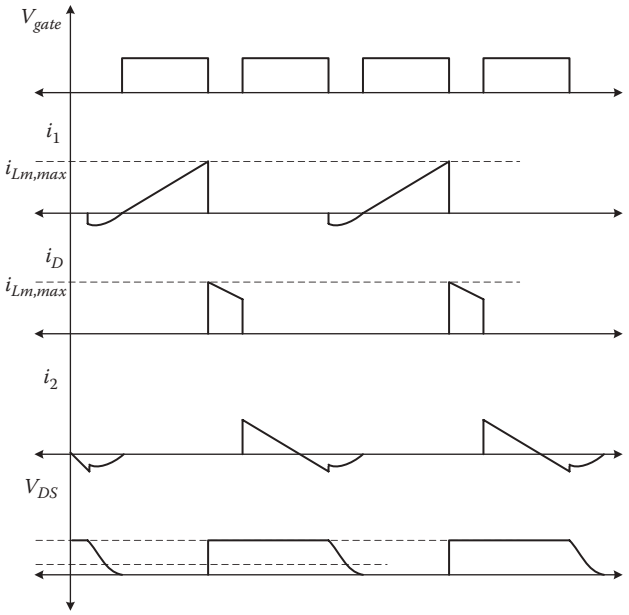


Figure 12.11 Operating waveforms for VF DCM ZVS synchronous flyback converter.

It should be noted that in the VF-ZVS-DCM flyback converter with the SR, the capacitive turn-on switching loss of the primary switch is traded off for the conduction loss. According to Figure 12.11, due to the negative secondary current, the RMS value of the secondary current is slightly increased. Therefore, the VF-ZVS converter in Figure 12.11 might not necessarily achieve higher efficiency compared to the VF converter with partial ZVS (Figure 12.10).

12.2 Synchronous Rectification in Forward Converter

A number of SR implementations have been described for the forward converter [9]–[16]. Based on the method employed in driving SRs, most of them can be broadly classified into two groups: control-driven and self-driven. In a control-driven SR implementation, the SRs are driven by gate drive signals derived from the gate drive of the main switch. In a self-driven SR implementation, the SRs are driven directly with the secondary voltage of the transformer. As a result, the self-driven SR approach is very attractive since it is simple and requires a minimum number of components. However, the performance of self-driven SRs depends on the

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resetting method of the power transformer since the reset voltage drives the freewheeling synchronous rectifier. Ideally, it would be desirable that the resetting time be equal to the off time of the primary switch. Then the output current will freewheel through the SR for the entire off (freewheeling) time.

The objectives of this section are two-fold. The first is to analyze the efficiency improvements that can be obtained from SRs. This limit is primarily a function of the output voltage, output current, on resistance of the SR, and the forward-voltage drop of Schottky rectifiers replaced by SRs. The second objective is to compare conversion efficiencies of control-driven SRs with those of different self-driven SR implementations. Specifically, performance comparisons of the forward converters with resistive-capacitive diode (RCD) clamp and active clamp reset are made in this section.

12.2.1 Forward Converter with RCD Clamp and Self-Driven SRs

The forward converter with self-driven SRs and its key waveforms are shown in Figure 12.12. In this circuit, synchronous rectifiers SR_1 and SR_2 are cross-coupled to the secondary winding of the transformer and are directly driven by the secondary voltage.

Since no driver or control circuit is used to provide the gate drive signals, this implementation of synchronous rectification is the simplest possible [17]. However, its performance is strongly dependent on the method of the transformer core resetting, because the gate drive signal for synchronous rectifier SR_2 is derived from the reset voltage (Figure 12.13).

As can be seen from the waveform in Figure 12.14, once the transformer reset is completed, the magnetizing current of the transformer starts flowing through the body diode of SR_1. Also, as can be seen from

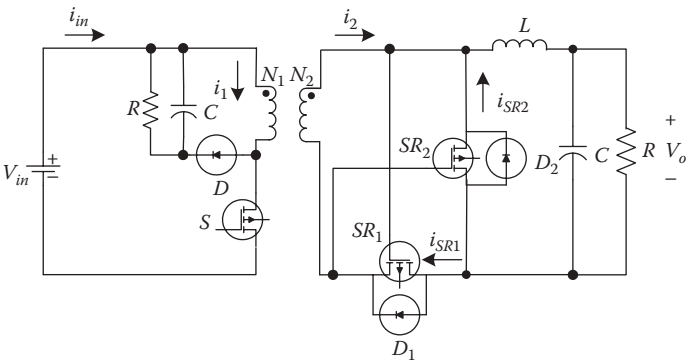


Figure 12.12 Self-driven synchronous forward converter with RCD clamp.

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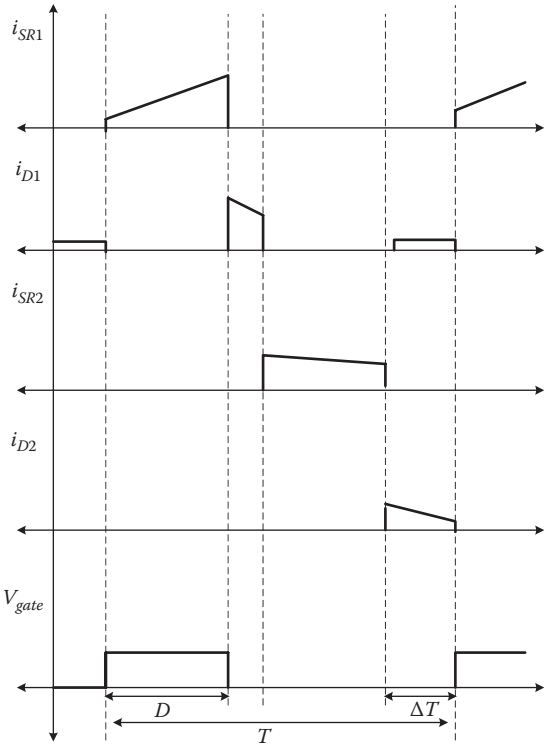


Figure 12.13 Waveforms of synchronous forward converter with passive clamp.

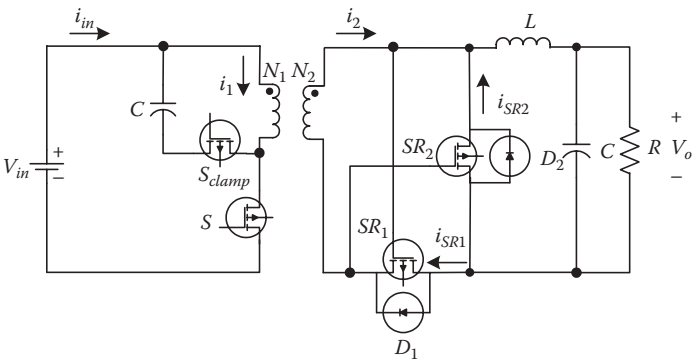


Figure 12.14 Self-driven synchronous forward converter with active clamp.

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the waveforms after the transformer reset is completed, the difference between load current and magnetizing current is diverted from transistor SR_2 to the body diode D_2. Due to relatively high forward voltage drops of the body diodes of SR_2 and SR_3, the efficiency of synchronous rectification is reduced.

The efficiency loss due to the body-diode conduction depends on the duration of the dead time and the forward voltage drops of the body diodes. This loss can be minimized by connecting Schottky diodes in parallel with SR_1 and SR_2. It can also be reduced by minimizing the conduction times of D_1 and D_2. While the conduction time of D_2 can be minimized either by driving SR_2 by an external gate drive signal or by minimizing the dead time by employing a different reset scheme, the conduction time of D_1 can be shortened only by employing a transformer reset scheme that minimizes the dead time. However, it must be noted that for load currents much greater than magnetizing current, the efficiency loss occurring during the dead time due to the conduction of D_2 is much greater than that of D_1.

12.2.2 *Forward Converter with Active Clamp and Self-Driven SRs*

The forward converter with active-clamp reset is shown in Figure 12.15. As can be seen, the active-clamp-reset approach minimizes the duration of the dead time since the transformer core is reset during almost the entire off time of the primary switch [18, 19]. As a result, the conduction time of MOSFET SR_2 is maximized, and the time during which D_1 is conducting magnetizing current is minimized.

Consequently, the conversion efficiency of the converter with the active-clamp reset is improved relative to the RCD-clamp counterpart.

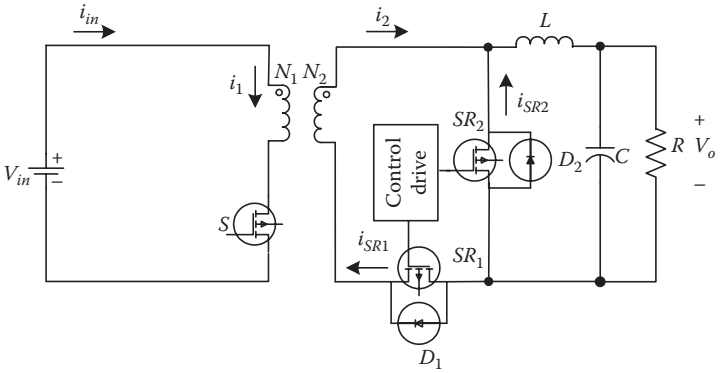


Figure 12.15 Control driven synchronous forward converter.

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Also, the active clamp reset approach minimizes voltage stress on the primary switch. In addition, the primary switch in this circuit can be turned on at zero voltage by properly adjusting the magnetizing inductance of the transformer [20]. However, the active clamp approach requires an extra switch and its associated gate drive, compared to the same circuit with the RCD-clamp reset. From this perspective, it is much simpler and more economical to use a Schottky diode in parallel with SR_1 to improve the efficiency of the RCD-clamp circuit than it is to implement the active clamp. Therefore, the active clamp approach is a viable choice in synchronous rectifier applications where voltage stress and soft switching are important design considerations (Table 12.2).

Generally, while self-driven SRs are simpler to implement, they are not suitable for applications with wide input-voltage variations. For the cross-coupled SRs shown in Figures 12.14 and 12.15, the maximum feasible input-voltage range depends strongly on the output voltage. For higher output voltages, the input-voltage range is narrower. Namely, the gate-drive voltage of SR_1 is proportional to the input voltage. Also, the minimum secondary (for example, gate-drive) voltage that occurs at low line is dependent on the desired output voltage and the maximum duty cycle. If the input-voltage range is wide (e.g., >3:1) and if the output voltage is relatively high (e.g., >5 V), the gate-drive voltage at the high line might exceed (or come close to) the maximum allowable gate-drive voltage. The effect of the output voltage on the amplitude of the gate-drive voltage can be eliminated by deriving the gate-drive signal for SR_1 from a separate winding. Also, the maximum gate-drive voltage can be limited by implementing a gate-to-source voltage-clamp circuit.

However, all these modifications require additional components and/or a transformer with an increased number of windings, which makes the self-driven approach more complex. Therefore, the self-driven SRs are best suited for applications with a relatively narrow voltage range (≤2:1) and low output voltage.

Table 12.2 Parameters for Forward Converter with Schottky Rectifier

Parameter	Value
Input voltage, V_{dc}	9
Switching frequency, f_s	50 k
Output voltage, V_{out}	1.5
Inductance, L_m	20 u
Capacitance, C	600 u
Turns ratio, n	1

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12.2.3 Forward Converter with Control-Driven SRs

The forward converter with control-driven SRs and its key waveforms are shown in Figures 12.16 and 12.17, respectively. In this circuit, MOSFETs SR_1 and SR_2 are driven by gate-drive signals derived from the primary switch gate drive [14]–[16]. As a result, the conduction times of the synchronous rectifiers are independent of the transformer resetting method [21], but solely depend on the timing of the gate-drive signals. However, as can be seen from Figure 12.17, while driving the SRs from the control circuit results in the maximum conduction time of SR_2, it has no effect on the conduction time of the magnetizing current through diode D_1 during the dead time [22]. Because MOSFET SR_1 is off during dead time, the conduction of diode D_1 during the dead time with control-driven SRs is exactly the same as for the self-driven SRs. Ideally, the gate-drive timing of SRs should allow no conduction of the body diodes of the SRs except for the unavoidable conduction of D_2 during the dead time. This is only possible with a very precise gate drive timing where the gate drive of one SR is applied or terminated at the same instant the gate-drive of the other SR is terminated or applied. In practical applications, this ideally complementary drive is not possible. Accidental, brief overlapping of the gate drive signals that turn on both SRs simultaneously would short the secondary,

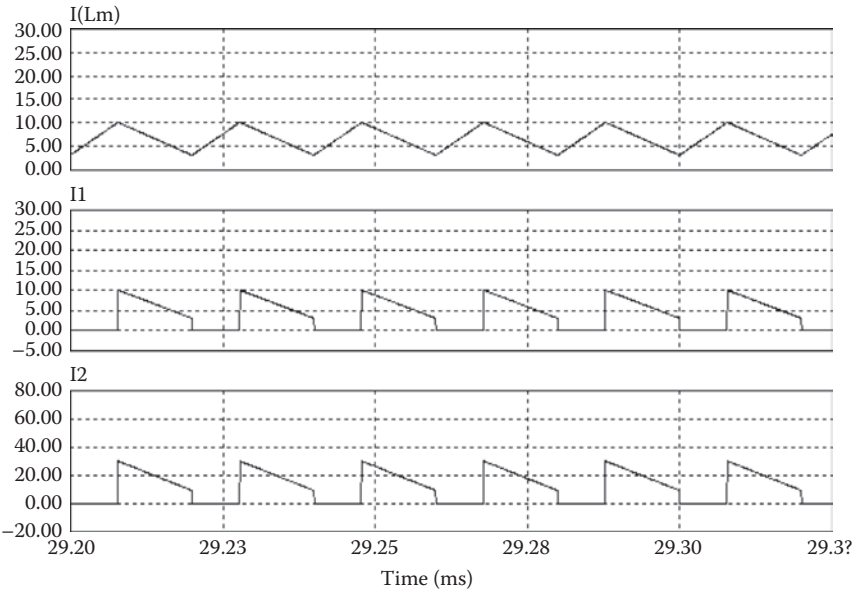


Figure 12.16 Simulated I(Lm), I1, and I2 for conventional flyback converter.

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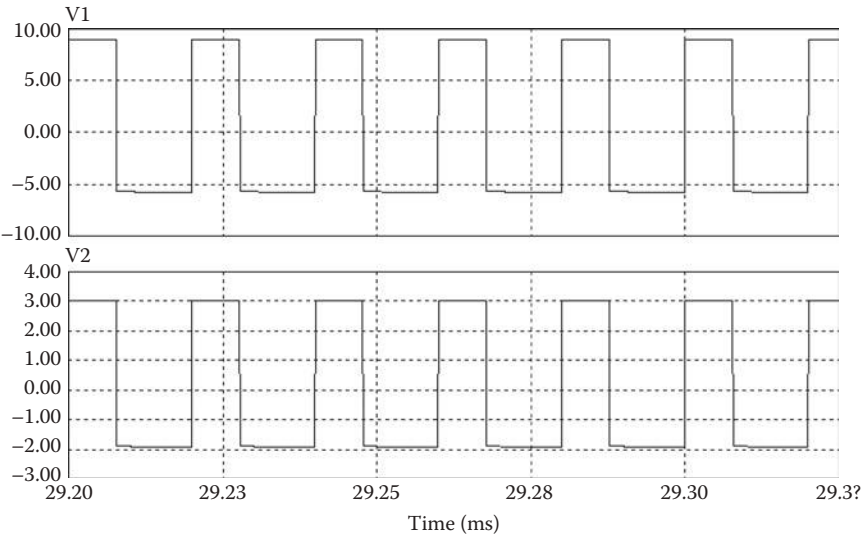


Figure 12.17 Simulated V1 and V2 for conventional flyback converter.

(causing an increased secondary current, and thus would lower efficiency or, in severe cases, would cause converter failure.

To avoid simultaneous conduction of SRs in practical applications, a delay between the gate-drive signals must be introduced. Since during the delay period no gate-drive signal is applied to the SRs, the body diodes of the SRs are conducting. This not only increases conduction loss but also introduces reverse recovery loss. Therefore, the performance of control-driven SRs is strongly dependent on the timing of the gate drive.

12.3 Simulation Results

To justify the theory presented above, the flyback converter is simulated for a 15 W, 1.5 V application. Both conventional and synchronous flyback converters are simulated and their performance is observed. Similarly, the forward converter is also simulated for a 1.5 V, 20 W application. Here also, both conventional and synchronous forward converters are simulated and results are observed. Figures 12.18 and 12.19 show operating mode current waveforms for the conventional flyback converter. Both of these waveforms closely match with the waveforms presented and expected theoretically in sections above.

From the simulated power loss for the flyback converter, average power loss is calculated. This power loss is around 8 W. As mentioned earlier, this converter is for a 15 W application, which means that the efficiency of the converter is around 50% [23].

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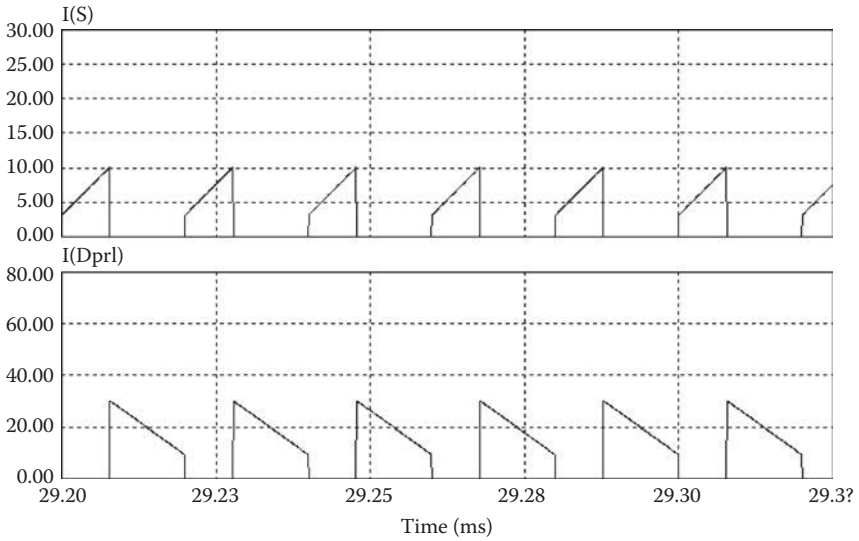


Figure 12.18 Simulated I(s) and I(Dpr1) for conventional flyback converter.

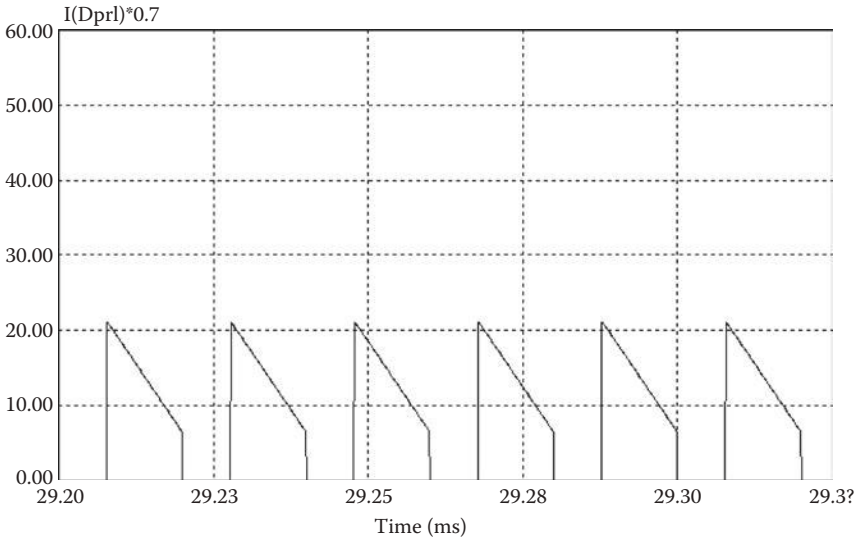


Figure 12.19 Simulated power losses in diodes for conventional flyback converter.

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From Figures 12.20–12.22, it can be said that the synchronous flyback converter operates exactly the same way as proposed theoretically and also similar to the conventional flyback converter.

From the simulated power loss, average power loss in the synchronous flyback converter is calculated (Figure 12.23). This power loss is 0.65 W. This means that the efficiency of the converter is 95.66%. Thus, 90% improvement in the efficiency can be achieved by this method.

From the simulated forward converter, average power loss is calculated (Figures 12.24 and 12.25). This power loss is around 10 W. This means the efficiency of the converter is around 50%.

From the simulated forward converter average power loss in all the switches is calculated, which is around 0.65 W. This gives an efficiency of 96%. This means that a 90% efficiency improvement can be achieved with synchronous rectification (Figures 12.26 and 12.27).

12.4 Summary

This chapter presented the theoretical efficiency improvement limits of various implementations of synchronous rectification in flyback converters. However, unlike synchronous rectification in the forward converter, it is difficult to normalize the efficiency improvement limit due to its complex dependence on several parameters. The VF DCM flyback converter implementation is most suitable for synchronous rectification. Moreover,

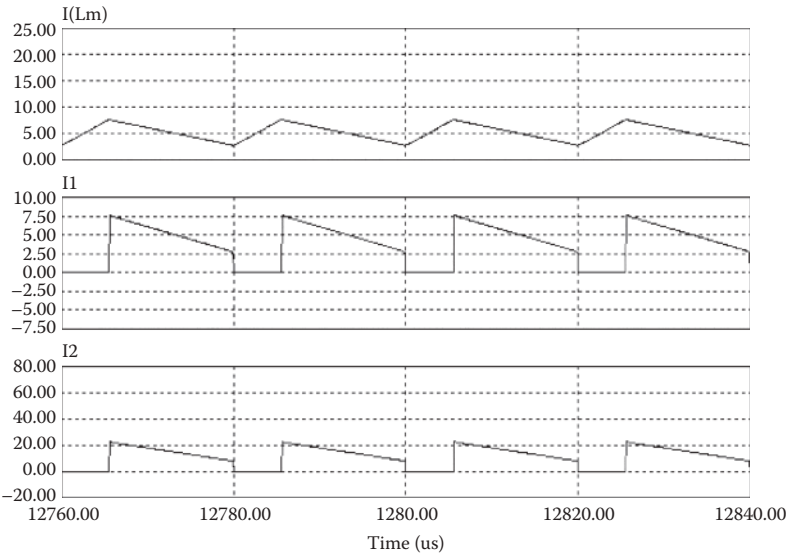


Figure 12.20 Simulated I(Lm), I1, and I2 for synchronous flyback converter.

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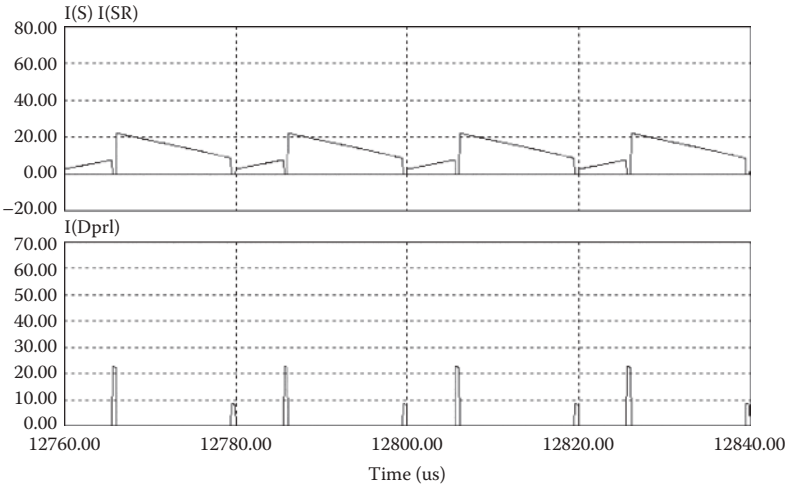


Figure 12.21 Simulated I(S), I(SR), I(Dpr1) for synchronous flyback converter.

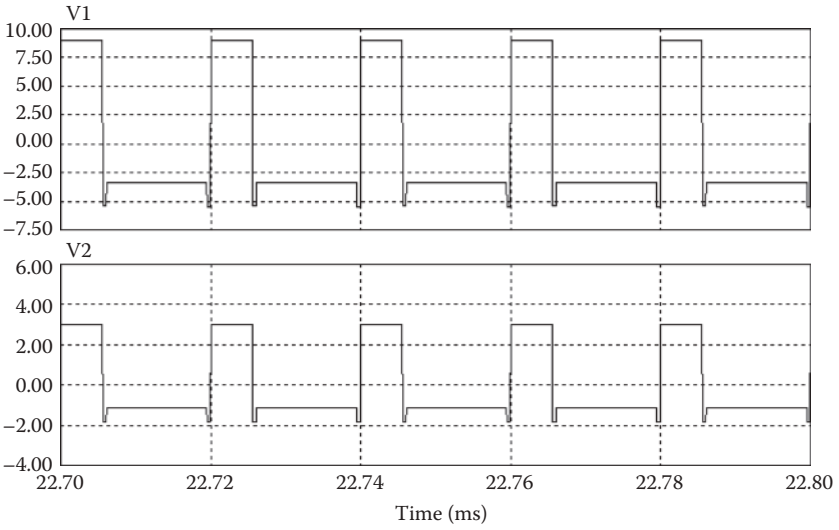


Figure 12.22 Simulated V1 and V2 for synchronous flyback converter.

this implementation can be easily designed to work with complete or partial zero voltage switching of the primary switch by properly adjusting the delay time between the zero crossing of the secondary current and the turn-off instant of the synchronous rectifier. In off-line applications, the VF DCM flyback converter with a synchronous rectifier shows a typical

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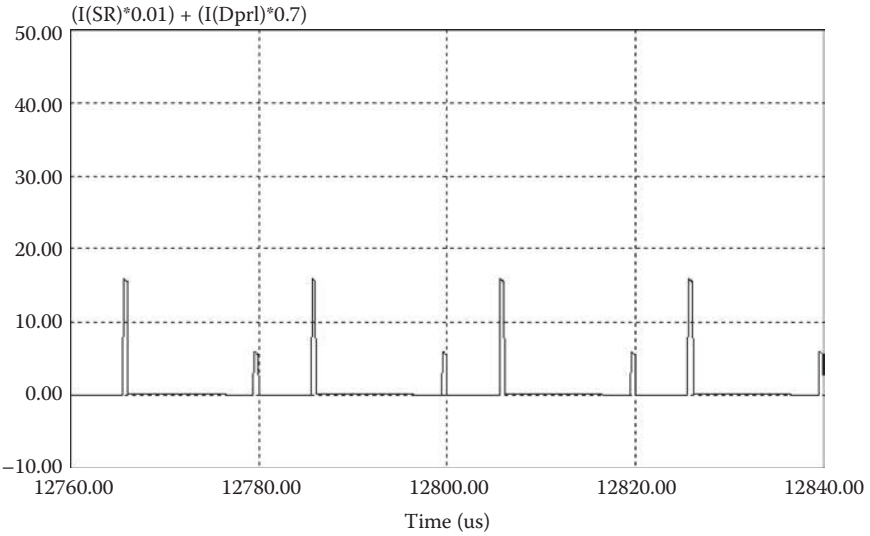


Figure 12.23 Simulated power losses in synchronous flyback converter.

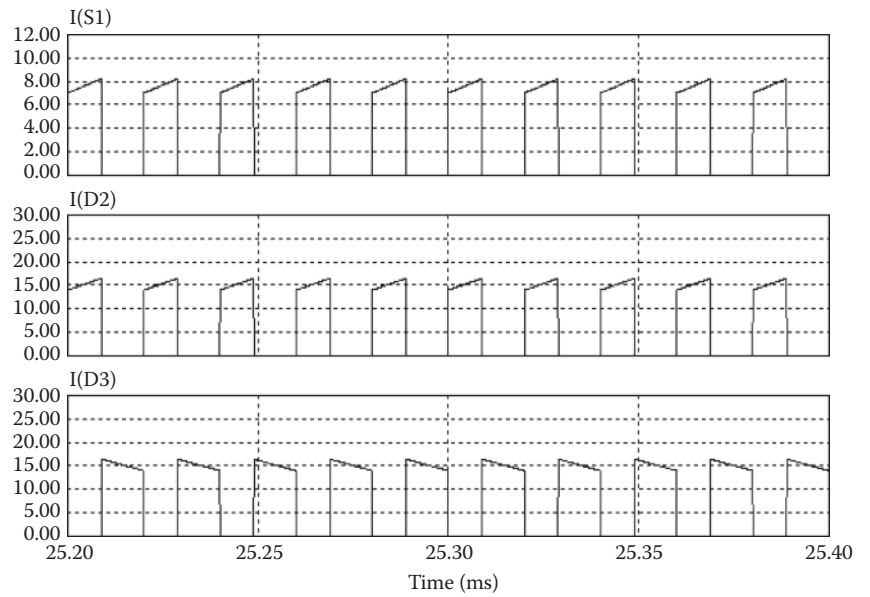


Figure 12.24 Simulated I(S1), I(D2), and I(D3) for conventional forward converter.

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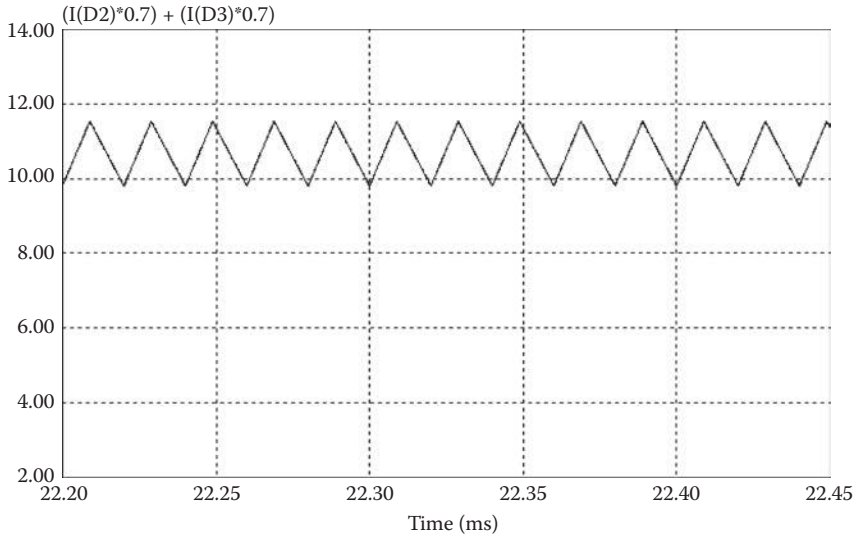


Figure 12.25 Power losses in conventional forward converter.

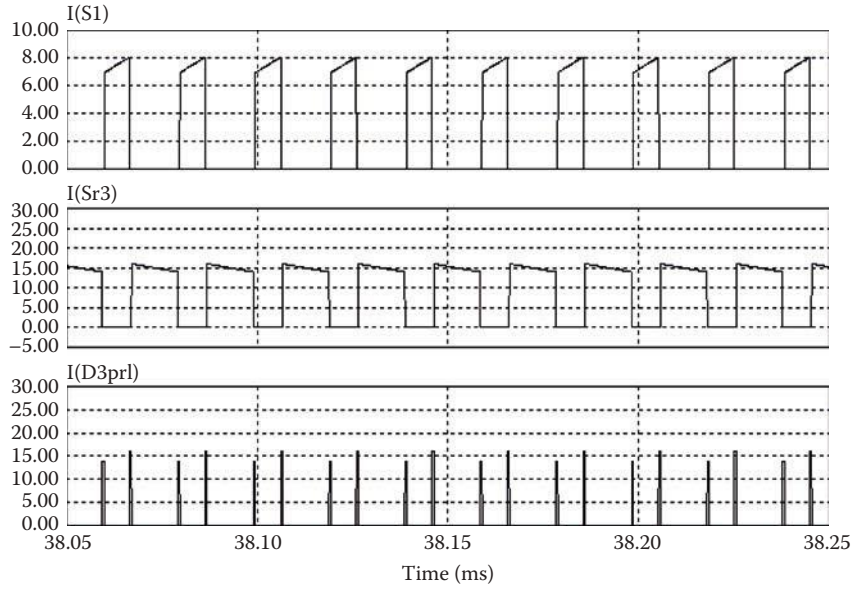


Figure 12.26 Simulated I(S1), I(Sr3), and I(D3prl) for synchronous forward converter.

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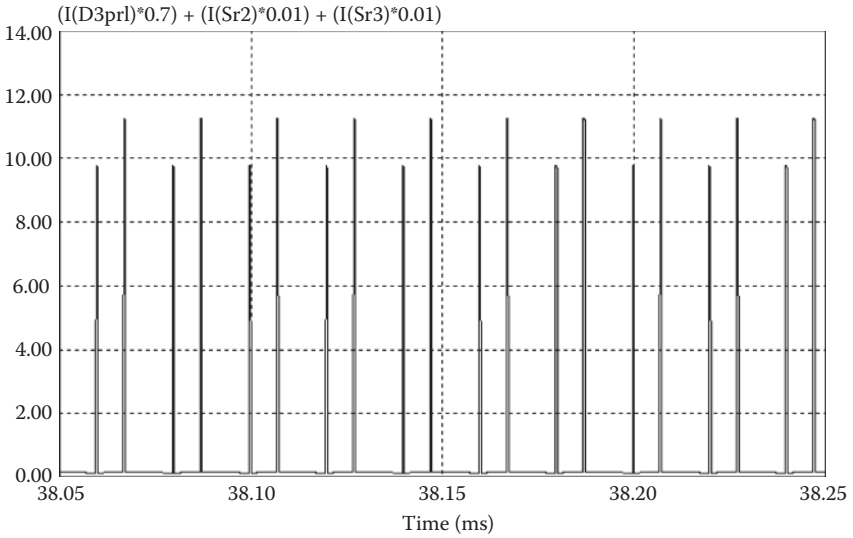


Figure 12.27 Simulated power losses in synchronous forward converter.

efficiency improvement in the 2%–4% range compared to the corresponding circuit with a diode rectifier.

Different implementations of synchronous rectification in the forward converter topology were discussed, and the effect of the transformer resetting mechanism on the performance of the self-driven SRs was analyzed. An estimate of the upper limit of the efficiency improvement of synchronous rectification relative to the Schottky diode implementation was explained. The limit is a function of the output voltage, output current, on-resistance of SRs, forward-voltage drop of Schottky devices replaced by SRs, efficiency of the converter, and SR implementation.

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chapter thirteen

Synchronous Rectification for Integrated High-Quality Rectifier-Regulators

For most of the switching power supply, two specification parameters are the key factors in deciding their market. One of them is efficiency and the other is the quality of power that it draws from the utility [1]–[4]. The efficiency improvement for power electronic applications at low power levels is achieved by replacing the diodes with MOSFETs. This is known as synchronous rectification. On the other hand, the quality can be improved by improving the power factor of the mains. By improving the power factor, the THD is improved and thus the quality is improved indirectly. In this chapter, new power electronic topologies are introduced that take care of both efficiency and quality.

In previous chapters, the importance of the power quality, the reasons for poor power quality, and the ways to improve the power quality were discussed. Various advanced power electronic topologies, for example, boost, buck, buck-boost, and flyback, were examined and analyzed for power factor correction. In Chapter 5 on integrated high-quality rectifier regulators (IHQRRs), it was concluded that these topologies serve most of the requirements of advanced switching power supplies. Similarly, the importance of efficiency improvement in advanced switching power supplies, the reasons for poor efficiency, and ways to improve the efficiency were discussed in previous chapters. Synchronous rectification is suggested as an effective method to improve the efficiency. This method of efficiency improvement was not studied and examined for the IHQRRs. This chapter analyzes the synchronous rectified IHQRRs. The topologies are proposed for the converters and their complete operation is also discussed. The merits and drawbacks of the proposed systems are presented. The control requirements for the proposed topologies are also described briefly. Finally, the other added features with the proposed topologies are outlined for further discussion.

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13.1 Synchronous Rectification for IHQRRs

Two topologies are discussed as IHQRRs: the boost integrated flyback rectifier/energy storage DC-DC converter (BIFRED) and boost integrated buck rectifier/energy storage DC-DC converter (BIBRED). From the theory of synchronous rectification, it is known that this technique mainly targets replacing the Schottky diodes with MOSFETs and by doing so achieving high efficiency. This is exactly what is done here. In the topologies of BIFRED and BIBRED, there are two Schottky diodes, for example, one on the primary side and one on the secondary side. Both of these diodes are replaced by MOSFETs and the same operating modes are achieved by proper control strategy [5]–[9].

13.1.1 Synchronous Rectified BIFRED

Figure 13.1 shows the conventional BIFRED, while its counterpart, the synchronous rectified BIFRED, is shown in Figure 13.2. In Chapter 4, it is mentioned that to achieve high power factor it is desirable to operate it in DCM-CCM mode (for example, input inductor in discontinuous conduction mode [DCM] and magnetizing inductance of the transformer in continuous conduction mode [CCM]). The same operating mode is achieved here.

The diodes in parallel of two synchronous rectifier MOSFETs, for example, SR_1 and SR_2, are Schottky diodes and they are provided here to conduct in the event of no conduction through the MOSFETs. These diodes are for dead time conduction. The detailed operation and operating mode description are presented in the following section.

13.1.2 Operation of Synchronous BIFRED

When the conventional BIFRED converter [10]–[12] is operated in DCM-CCM mode, one switching period consists of three sub-intervals. In the

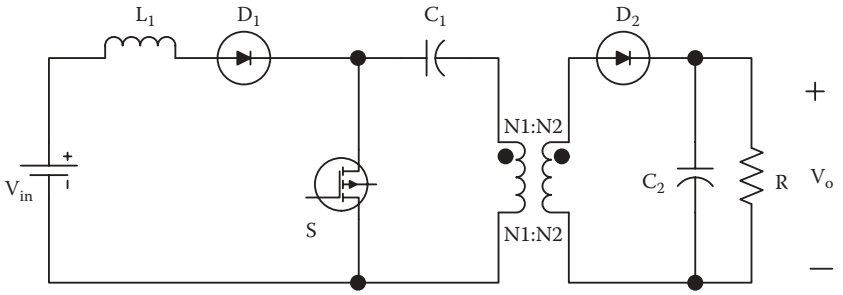


Figure 13.1 Conventional BIFRED converter.

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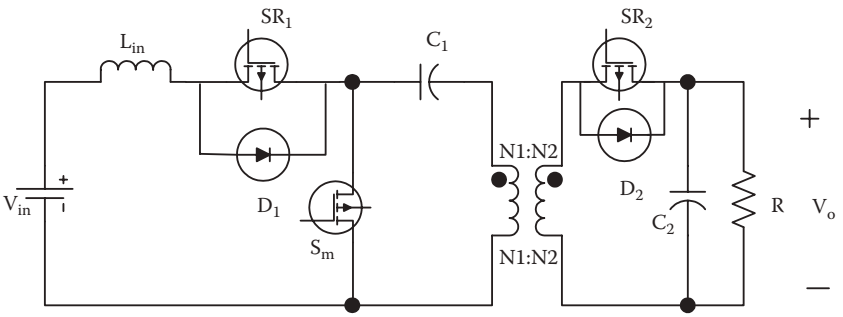


Figure 13.2 Synchronous BIFRED converter.

conventional BIFRED, only one controlled switch is available, and thus the uncontrolled switch, for example, input diode, forces the third mode. Here, with the proper control mechanism, the same operation has been achieved. Thus, the synchronous BIFRED converter has more subintervals in one switching period than the conventional one. Brief comments on control are given in a separate section. The first sub-interval starts when the main switch is made on. To let the input current go through the main switch and thus to the rest of the converter, the synchronous rectifier switch SR_1 has to be on simultaneously with the main switch. Due to this the current through the input inductor SR_1 and main switch S increases linearly. At this time the synchronous rectifier switch on the secondary side switch is off. The diode in parallel with it is reverse biased and thus it will also not conduct. The input side energy storage capacitor discharges linearly through the magnetizing inductance of the transformer. The magnetizing inductor current increases linearly. The power stage of the synchronous BIFRED in this sub-interval is shown in Figure 13.3.

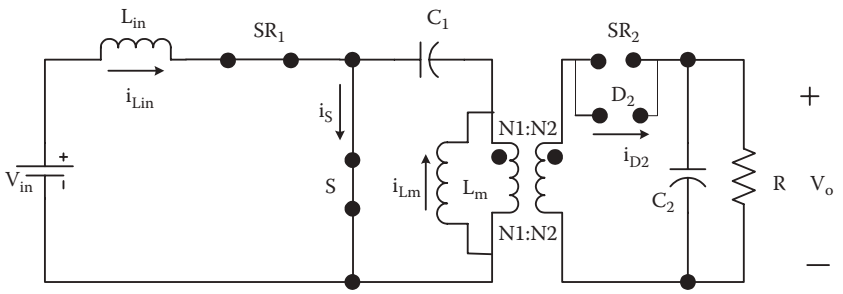


Figure 13.3 Synchronous BIFRED when S and SR_1 are on.

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As soon as the main switch is made off, the second sub-interval starts. In the conventional BIFRED, diodes are placed on the secondary side and in series with the input inductor.

And thus, when the main switch is off, the diodes conduct automatically. To achieve this here, we need to give the switch-on command to the synchronous rectifier MOSFET on the secondary side and input diode is already conducting. Both the main switch and the secondary side SR switch should not conduct simultaneously. To achieve this, the delay is provided between gate signals of both the switches. During this delay, the diode parallel to SR_2 is forward biased and it conducts. As the switch is turned off, the input inductor current starts decreasing and the energy storage capacitor starts charging. The magnetizing inductor current also decreases. The load is supplied from the input side and the output capacitor charges in this sub-interval through the diode D_2 in parallel with SR_2.

The power stage circuit diagram in this sub-interval is shown in Figure 13.4. Once the predefined delay is finished, the on command is given to the synchronous rectifier switch SR_2 on the secondary side. And the third sub-interval starts. In this sub-interval nothing is changed. The input inductor current and magnetizing continue to decrease. The energy storage capacitor continues to charge. The power stage of this sub-interval is shown in Figure 13.5. The only change that appears here is the transition from the diode to the synchronous rectifier.

This sub-interval comes to an end when the input inductor current reaches zero. The switch in series with the input inductor is bi-directional and thus the current can go negative. Due to this, as soon as the inductor current reaches zero, the synchronous rectifier switch SR_1 is turned off. The current cannot go negative and it stays at zero. On the other hand, the magnetizing inductor current continues to decrease. It must be noted that the converter is designed in such a way that the input inductor depletes its energy well before the magnetizing inductor.

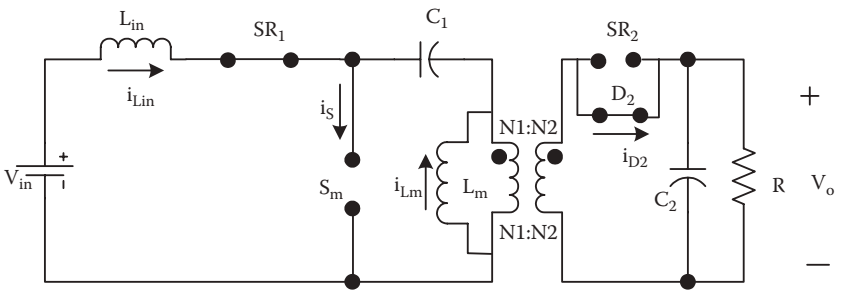


Figure 13.4 Synchronous BIFRED when main switch is off.

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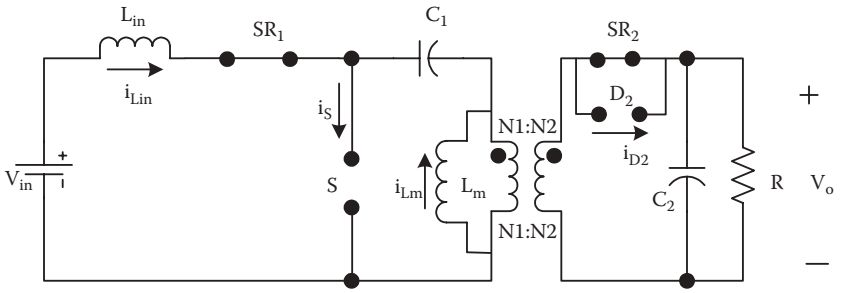


Figure 13.5 Synchronous BIFRED when SR_2 is on.

Even if there is a diode in parallel with this switch, it cannot conduct, as there is no current in the forward direction and diode cannot conduct in the reverse direction. Two changes occur in this sub-interval: the input inductor current goes to zero and the synchronous rectifier switch SR_1 stops conducting. The power stage circuit diagram for this sub-interval is shown in Figure 13.6.

When both the main switch and the synchronous rectifier SR_1 are off, the magnetizing inductor current continues to decrease. It must be kept in mind that the desired operating mode is DCM-CCM. Thus, any time before the magnetizing inductor current reaches zero, the main switch must be turned on. But, the synchronous rectifier switch SR_2 is conducting, and both S and SR_2 cannot be on at the same time. Thus, this sub-interval ends when SR_2 is turned off. The power stage circuit diagram for this sub-interval is shown in Figure 13.7.

As soon as the switch SR_2 is made off, the current transfers to the diode parallel to the SR_2. Current through the magnetizing inductor is still decreasing and has not reached zero. Again, it must be noted that the Schottky diode in parallel with the synchronous rectifier conducts

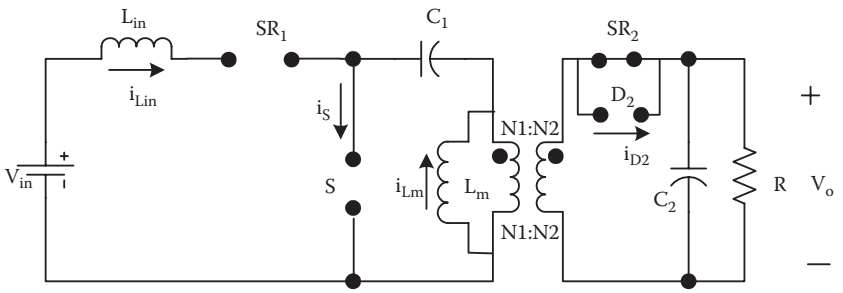


Figure 13.6 Synchronous BIFRED when SR_1 is off.

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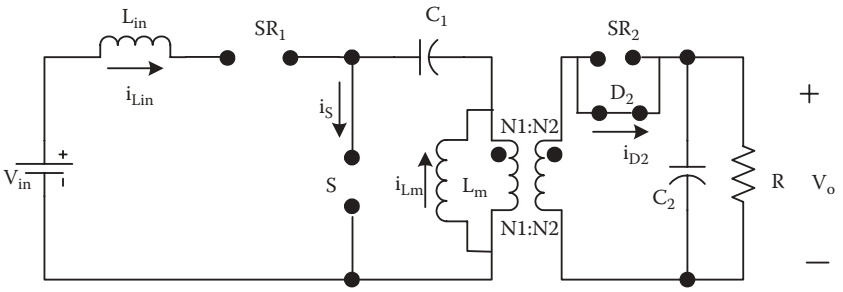


Figure 13.7 Synchronous BIFRED when all switches are off.

only during the dead times, when two active switches are not allowed to conduct simultaneously. Now, we can turn the main switch S on. Thus, this mode ends when the main switch is turned on again.

As soon as the main switch is turned on, the negative voltage appears across the diode on the secondary side and it will be off automatically. Thereafter, the cycle repeats itself. This completes one switching period and complete operation of the synchronous BIFRED converter. The operating mode waveforms are shown in Figure 13.8.

13.1.3 Synchronous Rectified BIBRED

Similar to the BIFRED, the other popular topology from the family of IHQRRs, BIBRED [13], can also be converted to a synchronous converter and efficiency improvements can be achieved. Figures 13.9 and 13.10 show a conventional BIBRED converter and asynchronous BIBRED converter, respectively.

The operation is the same as that of the BIFRED. Thus, the detailed operation of the converter is not discussed in this chapter, although the simulation results have been provided to confirm the efficiency improvement. The operating mode waveforms from the simulation results can be compared for the BIBRED with the waveforms presented in the Chapter 5 on IHQRRs.

13.2 Control of Synchronous IHQRRs

As can be seen from the power stage diagram of the synchronous BIFRED and synchronous BIBRED converters, these systems involve three active switches [14]-[26]. They all need their individual drivers and controls. This requires a very complex control strategy and three different drivers. The control of the converter can be as easy as that of the conventional IHQRR converters. Thus, any PWM, variable frequency, or phase-shift control can

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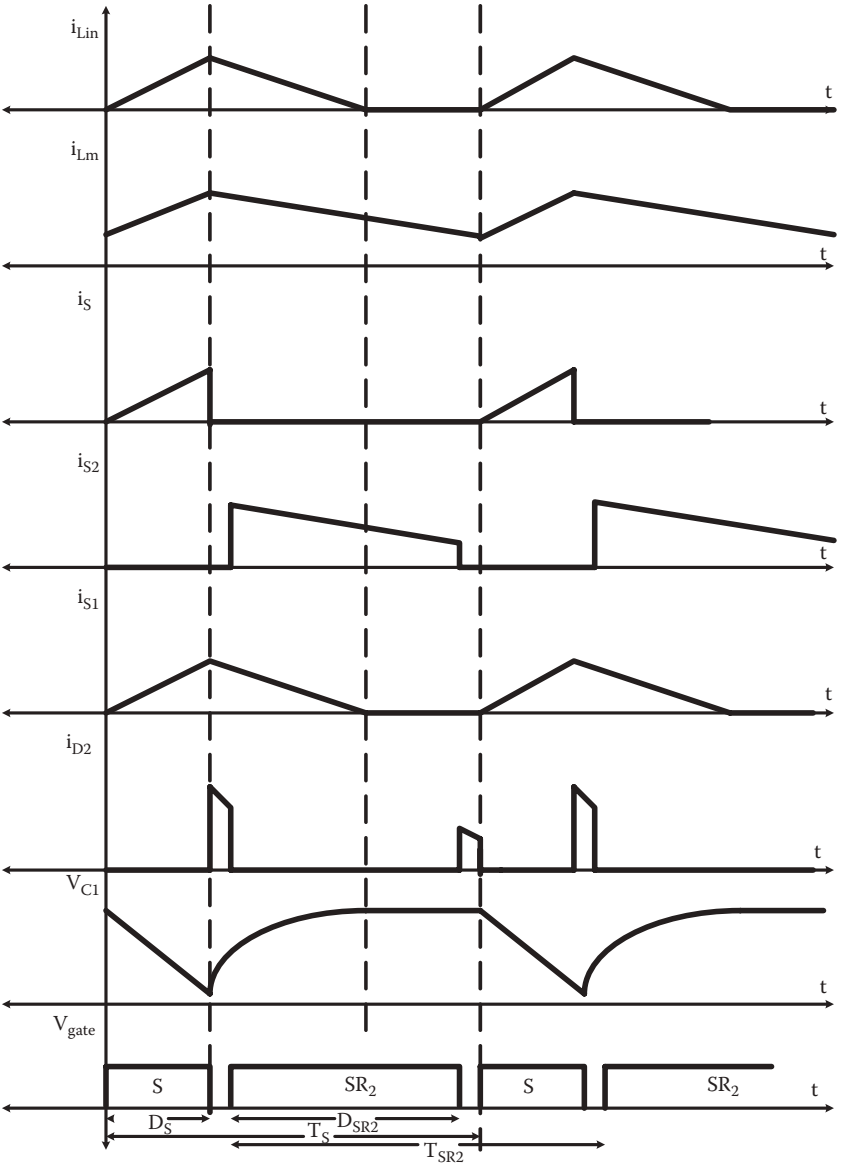


Figure 13.8 Operating mode waveforms for synchronous BIFRED.

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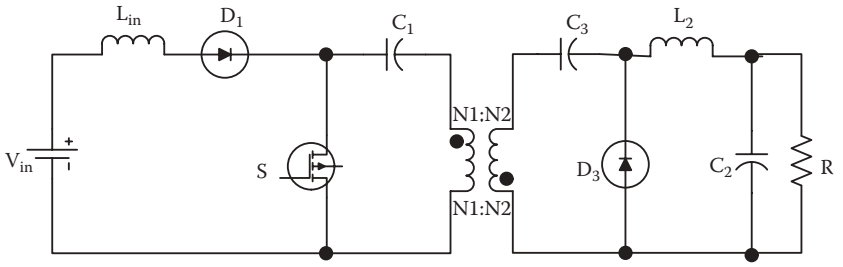


Figure 13.9 Conventional BIBRED converter.

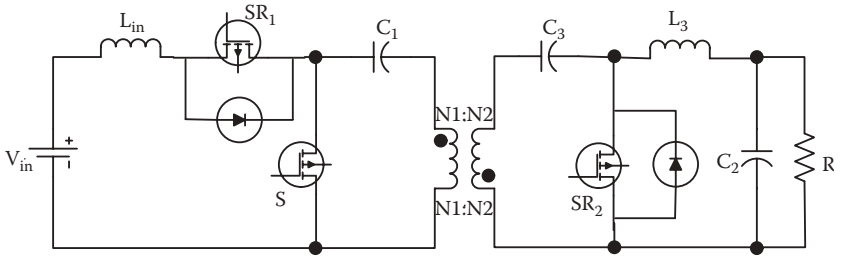


Figure 13.10 Synchronous BIBRED converter.

be applicable to the synchronous converter. This simplicity comes from the fact that the switch on the secondary side needs gating signals that are inversions of the gating signals of the main switch, though with some delay. This is the same for the synchronous buck, synchronous boost, or any conventional synchronous converter. Two MOSFETs with their drivers and controls built in an IC are also available. Now, if the input side synchronous switch SR_1 is considered, the turn on signal to this switch will be applied simultaneously with the main switch. Thus, it can come from the control and gating signal of the main switch. This means that no extra arrangements are needed to turn the primary side synchronous switch on. The turn-off signal must be given when the current through the input inductor reaches zero and tries to be negative. This can be easily implemented by using any simple flip-flop, which sets and resets the signal to the switch depending on the conditions mentioned above. It is also possible to calculate the time the input inductor needs to deplete its energy beforehand and the switch can be turned off at that time constantly. This can be incorporated in the same control IC used for the main switch. Thus, the cost or complexity of the controller and driver of the synchronous converter is not very high compared to their conventional counterparts. Continued improvements in the semiconductor industry enable

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us to use MOSFET, which has very low on-time resistance. The price of these MOSFETs is comparable with the ultra fast Schottky diodes.

13.3 General Efficiency Considerations of IHQRRs

The power losses in semiconductor switches can be of two types: switching losses and conduction losses. Synchronous rectification is the technique used to reduce the conduction losses. As explained and discussed in the chapter on synchronous rectification, the efficiency of the converter improves by replacing MOSFET with the conventional Schottky diode. Here also the same principle applies. If considering only the output side of the IHQRR converter, the average current through the output diode is the output or the load current. Thus, it can be written as

$$P_{D,Loss} = \langle i_o \rangle * V_D \tag{13.1}$$

where $P_{D,Loss}$ is the power loss due to the Schottky diode and V_D is the forward voltage drop across the diode, which is 0.5 to 0.7 V. Thus, it can be said that, as the load current increases, the loss in the Schottky diode increases. Also, for very low voltage applications, for example, 2 V, the loss of 0.5 V in the diode is very significant. On the other hand, if MOSFET is substituted in place of the diode, it can be written as

$$P_{SR,LOSS} = \langle i_o \rangle^2 * R_{DS,ON} \tag{13.2}$$

where $P_{SR,LOSS}$ is the power loss in the synchronous rectifier, for example, MOSFET, and $R_{DS,ON}$ is the MOSFET's on time resistance, which is less than 10 m for advanced MOSFETs available on the market. The power loss is extremely small in the case of MOSFET.

From this topology one can argue that as the number of switches is increased, the overall switching losses are high for these synchronous IHQRRs. This needs careful consideration, so let us look at the BIFRED converter here. If the primary side synchronous rectifier switch SR_1 is considered, this switch is made on and off at zero current through it. Thus, there is no switching loss for this switch. Similarly, the main switch is made on at zero current, and thus there is no switching loss during on time. If DCM-CCM mode is considered, we encounter some switching losses during off time. But if DCM-DCM operation is considered, where the energy storage capacitor discharges completely at every half switching period, the main switch can be made off at zero voltage. This will result again in zero switching losses. Again, the secondary side switch

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will turn on at zero voltage for DCM-DCM operation because the secondary side voltage is also zero. And due to DCM-DCM operation this switch is turned off at zero current. Thus, there is no switching loss at turn-off. Overall, there is not much switching loss and absolutely no increment of switching losses compared to its conventional counterpart converters.

13.4 Comparison of Power Losses in Schottky and Synchronous IHQRRs

The efficiency improvement that can be achieved by replacing Schottky rectifiers with synchronous rectifiers (SRs) is a complex function of many parameters. The most important are the output voltage, output current, SR on-resistance, forward voltage drop of Schottky diodes replaced by SRs, and efficiency of the converter with Schottky diodes in parallel with SRs. In this section, an estimate of overall efficiency improvements that can be achieved with SR implementation is presented.

Generally, the efficiency of a converter can be expressed as

$$\eta = \frac{P_o}{P_o + P_{loss} + P_{REC}} \tag{13.3}$$

where P_o is the output power, P_{loss} is the total loss excluding the rectifier loss, and P_{REC} is the rectifier loss.

For the converter with Schottky rectifiers, the efficiency can be given by

$$\eta_{SCH} = \frac{P_o}{P_o + P_{loss} + P_{SCH}} \tag{13.4}$$

Similarly, for the same converter with SRs, the efficiency can be given by

$$\eta_{SR} = \frac{P_o}{P_o + P_{loss} + P_{SR}} \tag{13.5}$$

Estimating P_{loss} from the above equations, the efficiency of the converter with SRs can be expressed as a function of the efficiency of the converter with the Schottky diodes,

$$\eta_{SR} = \frac{P_o}{P_o / \eta_{SCH} - P_{SCH} + P_{SR}} \tag{13.6}$$

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The power loss in the Schottky is a very simple function of forward voltage drop and current through it:

$$P_{SCH} = V_{SCH} * I_{SCH} \tag{13.7}$$

where V_{SCH} is the forward voltage drop of the Schottky diode and I_{SCH} is the current through it.

For the BIFRED converter two Schottky rectifiers are replaced by two SRs. One of them is on the input side, that is, the boost side, and the other is on the output side, that is, the flyback side. In a conventional BIFRED converter, the input side diode conducts for an almost complete cycle of switching period. For the synchronous rectifier BIFRED, MOSFET also conducts for a complete switching period. There is no delay between the gating signal of the main switching MOSFET and the synchronous rectifier MOSFET. Thus, it is not necessary to have a Schottky diode in parallel with the synchronous rectifier MOSFET. Thus, for the BIFRED with a Schottky diode, the power loss in the input stage Schottky rectifier is given by

$$P_{SCH,in} = V_{SCH,in} * I_{in} \tag{13.8}$$

where $V_{SCH,in}$ is the forward voltage drop of the input side Schottky rectifier and I_{in} is the average input current.

On the other hand, power loss in the counterpart SR in BIFRED is given by

$$P_{SR,in} = \left(R_{DS(on)} * I_{in}^2\right) + \left(V_D * I_{in} * D_{dead}\right) + \left(P_{RREC}\right) + \left(P_{gate}\right) \tag{13.9}$$

$$D_{dead} = \frac{T_{dead}}{T_s} \tag{13.10}$$

where $R_{DS(on)}$ is the on time resistance of MOSFET, I_{in} is the averaged input current, V_D is the voltage drop of the diode in parallel with SR, D_{dead} is the dead time duty cycle during which this diode conducts, P_{RREC} is the diode recovery loss, and P_{gate} is the power loss in gate driver of the MOSFET, which is substituted as SR.

As there is no need for a diode in parallel with the input SR, the power loss in input SR can be given by

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$$P_{SR,in} = \left(R_{DS(on)} * I_{in}^2\right) + \left(P_{gate}\right) \tag{13.11}$$

It must be noted that all the equations are derived assuming that commutation times are zero and the effect of magnetizing inductance as well as leakage inductance is not considered. Therefore it can be said that

$$T_{Comm}^{on} = T_{Comm}^{off} = 0 \tag{13.12}$$

$$I_{leakage} = 0 \tag{13.13}$$

Thus, it can be seen that the power loss in primary side Schottky and SR is not a complex function, but for the output side (secondary side) of the converter the power loss function is much more complex.

The gating signals for the main switch on the primary side and the SR switch on the secondary side are complementary. For proper operation of the BIFRED converter, care must be taken that both the signals do not overlap. To achieve this feature, definite dead time is provided between both of the gating signals. During this time, the current must pass through some other path. Therefore, the diode must be placed in parallel with the output side SR.

Considering the above facts, if the BIFRED converter with Schottky rectifier is implemented, the power loss in the output side Schottky is given by

$$P_{SCH,out} = P_{SCH,out}^{cond} + P_{SCH,out}^{sw} + P_{SCH,out}^{cap(sw)} \tag{13.14}$$

where P^{cond} is the conduction loss component, P^{sw} is the switching loss component, and P^{cap} is the capacitive turn-on switching loss of the primary switch. The individual terms can be given by

$$P_{SCH,out}^{cond} = V_{f,SCH} * I_o \tag{13.15}$$

$$P_{SCH,out}^{sw} = P_{off} + P_{RR} = \frac{C_T}{2}\left(V_o + \frac{V_{in}}{n}\right)^2 + Q_{RR}\left(V_o + \frac{V_{in}}{n}\right) * f_s \tag{13.16}$$

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$$P_{SCH,out}^{cap(sw)} = \frac{C_{oss}^{sw}}{2}\left(V_{in} + nV_o\right)^2 * f_s \tag{13.17}$$

where $V_{f,SCH}$ is the forward voltage drop of the Schottky diode, I_o is the average output current, C_T is the total capacitance reflected on the secondary side of the transformer, V_o is the output voltage, V_{in} is the input voltage, n is the transformer turns ratio, f_s is the switching frequency, and C_{oss} is the total output capacitance of the primary side switch. Summation of all of these components gives the power loss in the output side Schottky rectifier in BIFRED.

On the other hand, if SR replaces the output side Schottky, the power loss in SR can be given by

$$P_{SR,out} = P_{SR}^{cond} + P_{SR}^{sw} + P_{SR}^{cap(sw)} \tag{13.18}$$

Similar to the Schottky rectifiers, the individual terms in the above equation for SR are given by

$$P_{SR,out}^{cond} = R_{DS(on)} * \frac{I_o^2}{1-D} + \left(V_D * I_D\right) * \left(T_D^{off} + T_D^{on}\right) * f_s \tag{13.19}$$

$$P_{SR,out}^{sw} = P_{off} + P_{RR} = \frac{C_{oss}^{SR}}{2}\left(V_o + \frac{V_{in}}{n}\right)^2 + Q_{RR}^{SR}\left(V_o + \frac{V_{in}}{n}\right) * f_s \tag{13.20}$$

$$P_{SR,out}^{cap(sw)} = \frac{C_{oss}^{sw}}{2}\left(V_{in} + nV_o\right)^2 * f_s \tag{13.21}$$

where $R_{DS(on)}$ is the on time resistance of the MOSFET on the secondary side of the BIFRED, D is the duty ratio with respect to output current, I_o is the output current (which is continuous), V_D is the forward voltage drop across the Schottky connected in parallel with the SR, I_D is the current through the same Schottky, T_{off} and T_{on} are the commutation time during which the parallel Schottky conducts, C_{oss} is the output capacitance of the synchronous rectifier MOSFET, and Q_{RR} is the reverse recovery charge of the synchronous rectifier.

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Considering that these are the dominant components of the losses in both Schottky rectifiers and synchronous rectifiers, the relative efficiency can be compared as

$$\frac{\eta_{SR}}{\eta_{SCH}} = \frac{P_{SR,in} + P_{SR,out}}{P_{SCH,in} + P_{SCH,out}} \tag{13.22}$$

From the above equation percentage efficiency improvement can be obtained. It is important to note that the BIFRED converter is analyzed for DCM-CCM mode. Thus, input SR is in DCM and output SR is in CCM. This not an exact loss analysis, but an estimate of losses. Many parameters, such as magnetizing inductance, leakage inductance, and difference in MOSFET on time resistances, are not taken into consideration.

13.5 Simulation Results and Observations

The theoretical analysis presented above is verified with the simulation results. A BIFRED converter for a 2 V, 40 W application with 9 V input is simulated for both conventional and proposed synchronous topologies. The simulation results are shown in Figures 13.11–13.13.

Parameters shown in Table 13.1 remain exactly the same for both the Schottky rectifier BIFRED and the synchronous BIFRED.

As mentioned earlier, for a 40 W, 2 V application the conventional BIFRED converter is simulated and results are observed. If average power loss is considered across the diodes it comes out to be around 20 W. Thus, for a 40 W application, the efficiency is 50%.

On the other hand, when the synchronous BIFRED converter is simulated and the power loss in all the MOSFETs and all the parallel diodes is considered, the average loss is 2 W. This gives an efficiency of 95%, which means that a 90% improvement in the efficiency can be achieved by employing synchronous rectification. From the simulation results shown in Figures 13.14–13.16 for the synchronous BIFRED converter, it can be said that the performance remains the same, that is, quality improvement.

Now let us consider a 1.5 V, 20 W application of a BIBRED converter. Both conventional and synchronous BIBRED converters are simulated and the results are analyzed (Table 13.2). All other components in both conventional and synchronous converters are the same. Only diodes are replaced by the MOSFET (Figure 13.17).

The waveforms for power loss in the diodes are given in Figure 13.18. The average power loss turns out to be 11 W. For a 20 W application, this means an efficiency of 50% again (Figure 13.19).

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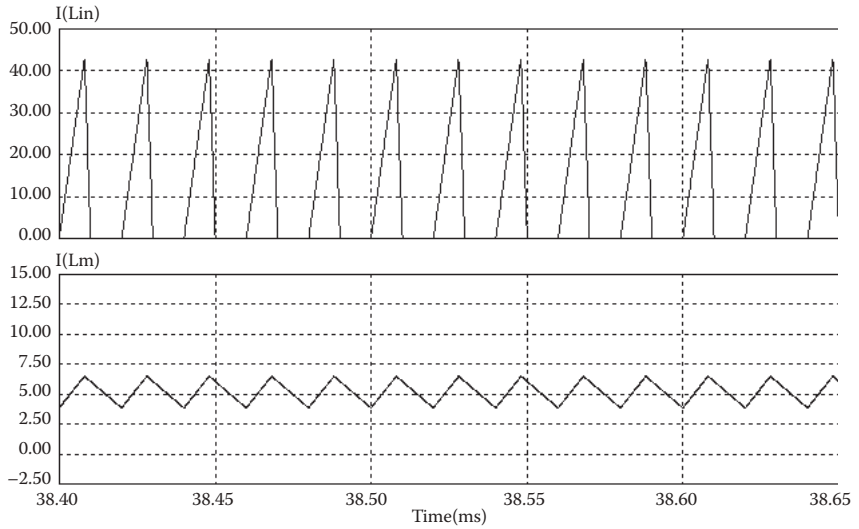


Figure 13.11 Simulated I(Lin) and I(Lm) for conventional BIFRED.

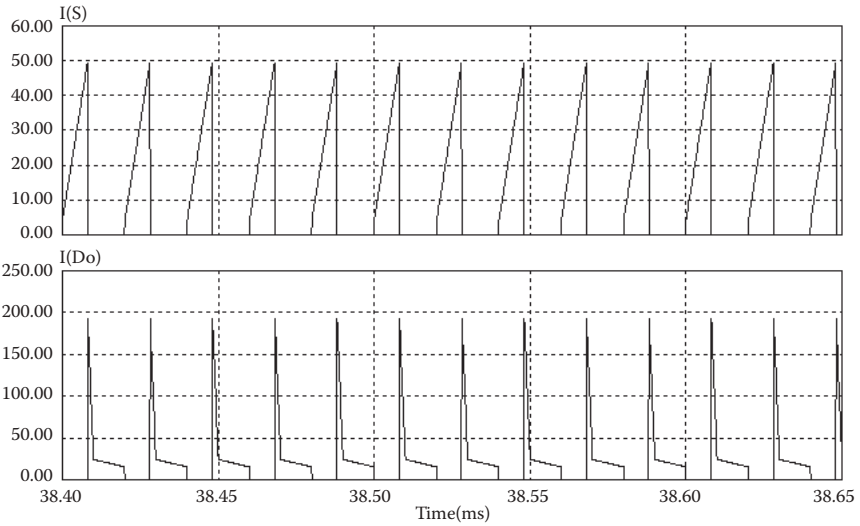


Figure 13.12 Simulated I(S) and I(Do) for conventional BIFRED.

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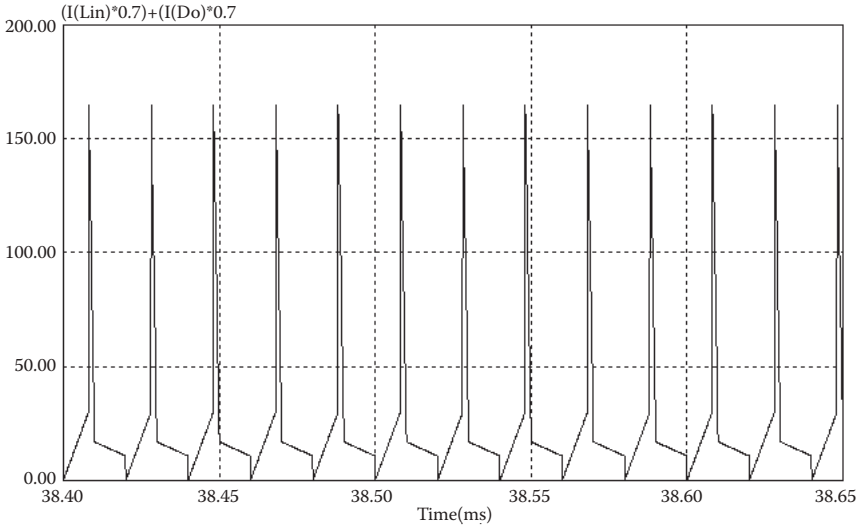


Figure 13.13 Power losses in all the diodes of conventional BIFRED.

Table 13.1 Parameters for BIFRED Converter with Schottky Rectifier

Parameter	Value
Input voltage, V_{in}	6
Switching frequency, f_s	50 k
Output voltage, V_{out}	2
Inductance, L_{in}	10 u
Inductance, L_{in}	50 u
Capacitance, C_1	50 u
Capacitance, C_o	500 u
Turns ratio, n	1

The main switch current, synchronous switch current on the secondary side, and the current through the diode parallel to the synchronous switch are shown in Figure 13.20.

From the power loss waveforms shown in Figure 13.21, the average power loss in the synchronous BIBRED converter is calculated. This power loss is around 0.85 W. For a 20 W application, with an efficiency of 95.75%. On the other hand, for the conventional BIBRED converter, the loss was around 50%. This means that an efficiency improvement of around 90% can be accomplished by employing synchronous rectification for these converters. The theoretically expected operating mode waveforms are

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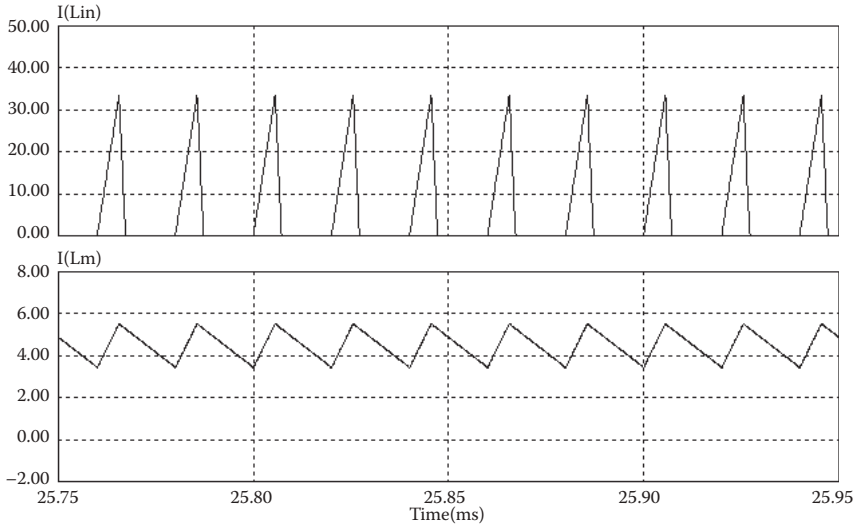


Figure 13.14 Simulated I(Lin) and I(Lm) for synchronous BIFRED.

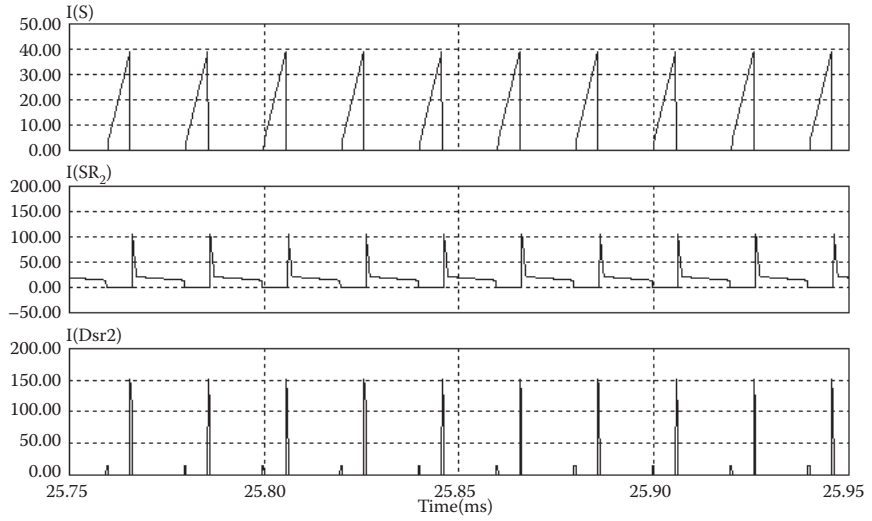


Figure 13.15 Simulated I(S), I(SR_2), and I(Dsr2) for synchronous BIFRED.

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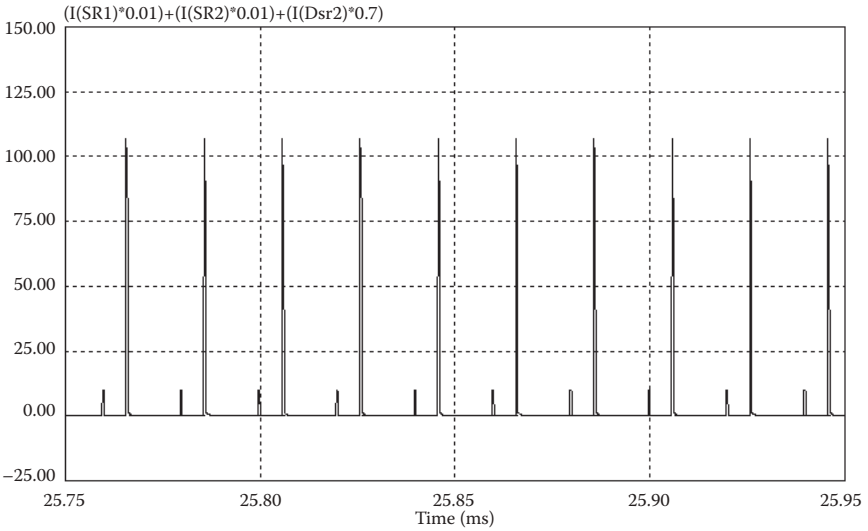


Figure 13.16 Power losses in synchronous BIFRED.

Table 13.2 Parameters for BIBRED Converter with Schottky Rectifier

Parameter	Value
Input voltage, V_{in}	12
Switching frequency, f_s	50 k
Output voltage, V_{out}	2
Inductance, L_{in}	50 u
Inductance, L_m	180 u
Inductance, L_o	100 u
Capacitance, C_1	150 u
Capacitance, C_2	10 u
Capacitance, C_o	500 u
Turns ratio, n	1

similar to the results obtained from the simulations. This means that the theory presented here is justified and can be applicable practically.

13.6 Summary

In this chapter a new family of converters is introduced: synchronous rectified integrated high-quality rectifier-regulators. The synchronous rectification method is applied to two of the most popular topologies of the IHQRR family, BIFRED and BIBRED. The operating principle and complete operation are discussed for the BIFRED. The same operation can be

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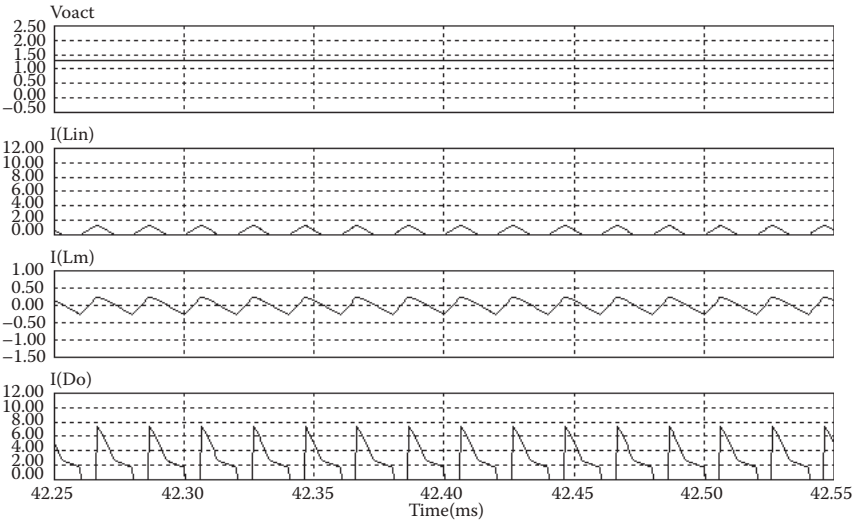


Figure 13.17 Simulated Voact, I(Lin), I(Lm), and I(Do) for conventional BIBRED.

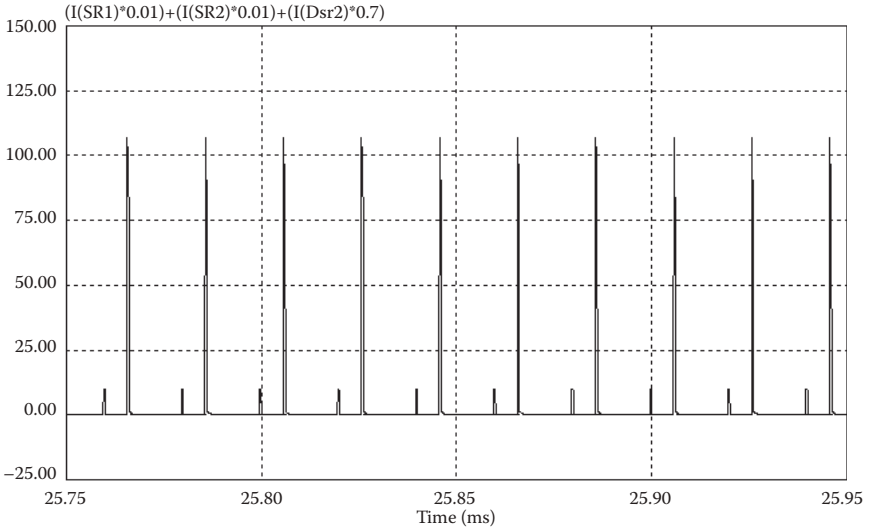


Figure 13.18 Power loss in conventional BIBRED.

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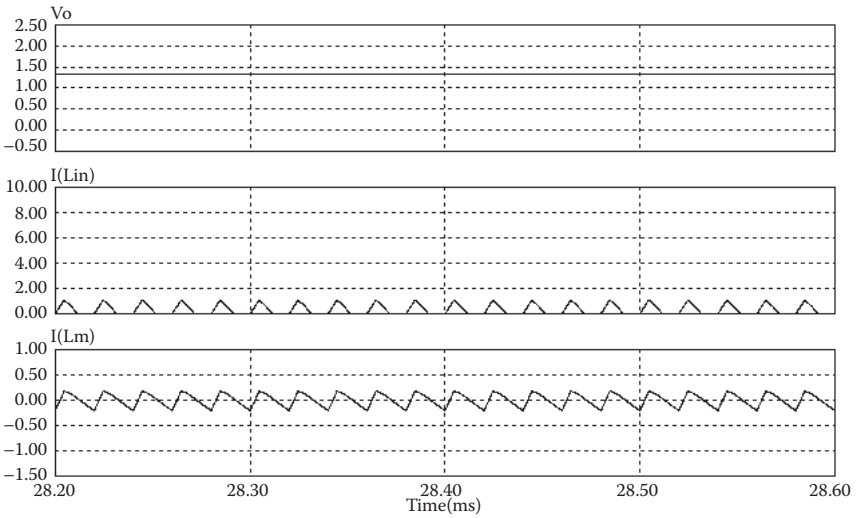


Figure 13.19 Vo, I(Lin), and I(Lm) for synchronous BIBRED.

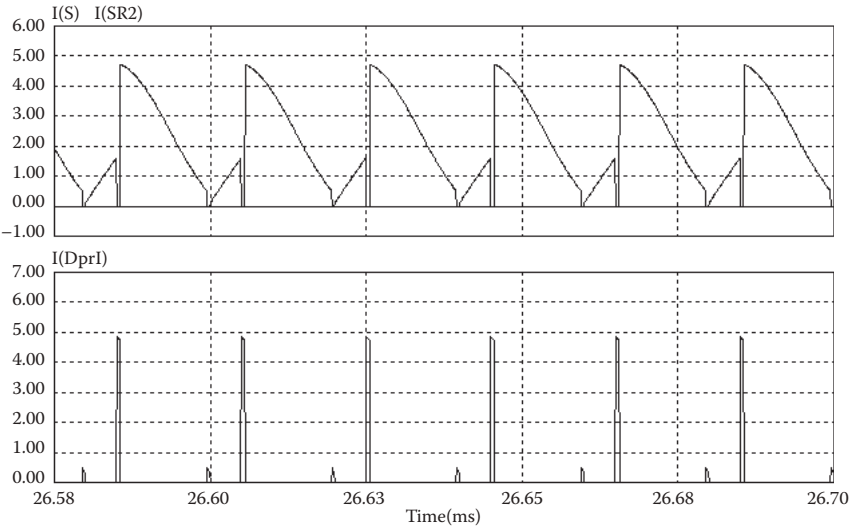


Figure 13.20 I(S), I(SR_2), and I(Dpr1) for synchronous BIBRED.

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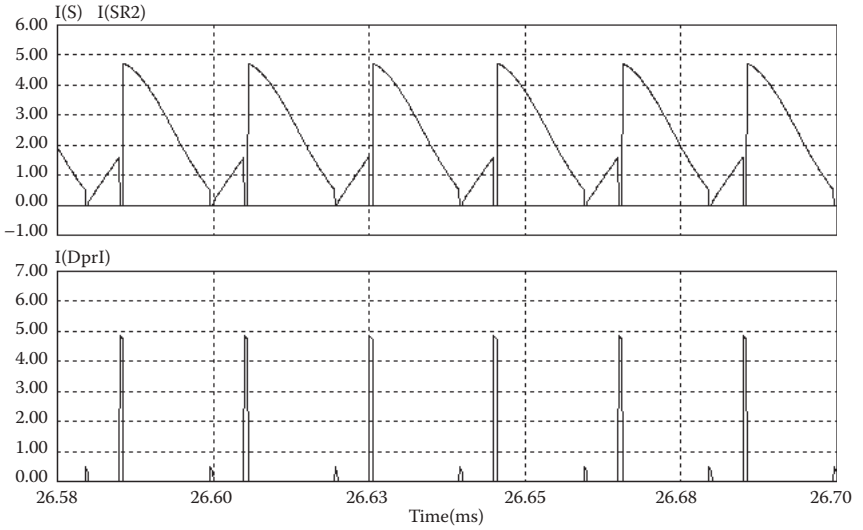


Figure 13.21 Power loss in synchronous BIBRED.

achieved for the synchronous BIFRED as for conventional BIFRED. High quality can be kept intact and the efficiency feature can be added by introducing synchronous rectification to this family of IHQRRs. Considerable efficiency improvements are predicted theoretically and achieved in simulations. Both BIFRED and BIBRED converters are simulated and results are closely matched with the proposed theoretical results.

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chapter fourteen

Integrated Switched-Mode Power Supplies Applications

14.1 Integrated Switched-Mode Power Converters for UPS Applications

Uninterruptible power supply (UPS) systems provide reliable, and high-quality power for vital loads. In fact, they protect sensitive loads against power outages as well as over-voltage and under-voltage conditions. UPS systems also suppress line transients and harmonic disturbances. Applications of UPS systems include medical facilities, life supporting systems, data storage and computer systems, emergency equipment, telecommunications, industrial processing, and on-line management systems [1]–[3].

Generally, an ideal UPS should be able to deliver uninterrupted power and simultaneously provide the necessary conditioning for a particular power application. Therefore, an ideal UPS should have the following features: regulated sinusoidal output voltage with low total harmonic distortion (THD) independent from the changes in the input voltage or in the load, on-line operation that means zero switching time from normal to backup mode and vice versa, low THD sinusoidal input current and near unity power factor, high efficiency, low EMI and acoustic noise, electric isolation, low maintenance, and low cost, weight, and size.

The main advantages of on-line UPS systems are very wide tolerance to the input voltage variation and very precise regulation of the output voltage. In addition, there is no transfer time during the transition from normal to stored energy mode. Figure 14.1 shows the conventional on-line UPS system. The main disadvantages of the conventional topology are low power factor, high THD at the input, and low efficiency. The rectifier destroys the input current unless an extra power factor correction (PFC) circuit is added, but this adds to the cost of the UPS system. Furthermore, the low-frequency transformer increases the cost for its big size and weight in low power applications.

Integrated high-quality rectifier-regulator (IHQRR) topologies consist of a discontinuous conduction mode (DCM) boost converter integrated with a second conversion stage. This kind of new family of AC/

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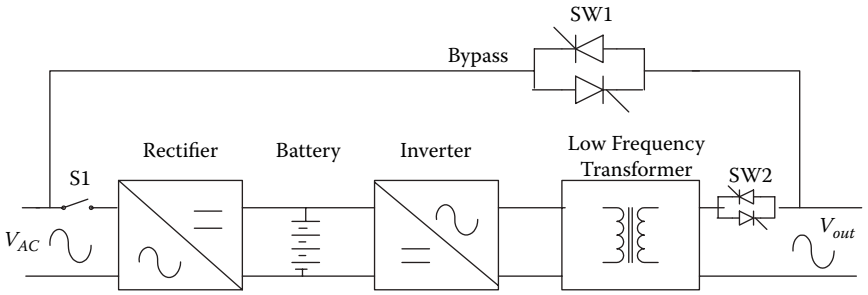


Figure 14.1 Conventional on-line UPS system.

DC converters offers a low-cost alternative to achieve power factor correction, fast dynamic response, and a desired output voltage regulation. Figure 14.2 presents the proposed UPS system. It consists of an IHQRR at the front end, a full-bridge DC/AC inverter at the back end, a battery charger/discharger, and a battery bank. The controlled output capacitor voltage from the IHQRR provides an almost constant DC link voltage for the inverter [1]–[7].

The boost integrated flyback rectifier/energy storage DC-DC (BIFRED) converter, which is a member of the IHQRR, consists of a DCM boost converter integrated with a DCM flyback converter as the second conversion stage. The controlled DC link voltage from the output capacitor of the

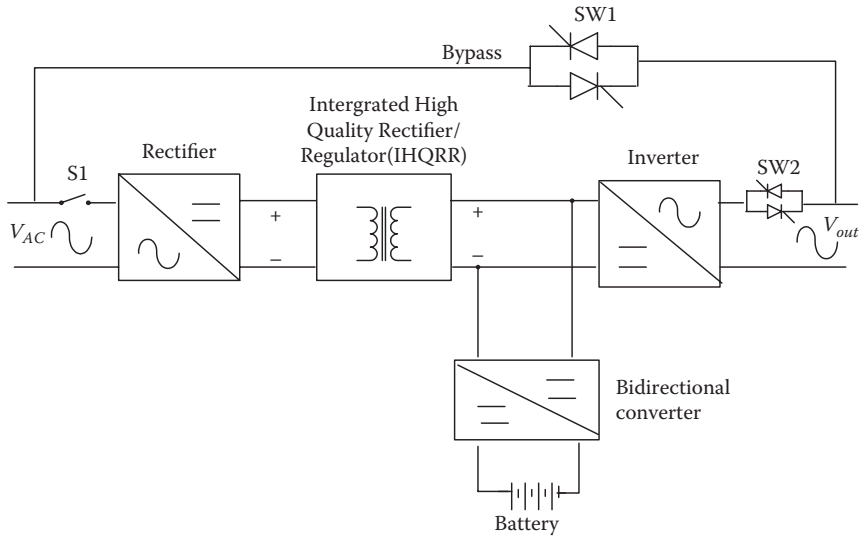


Figure 14.2 Proposed on-line UPS system with integrated rectifier-regulator.

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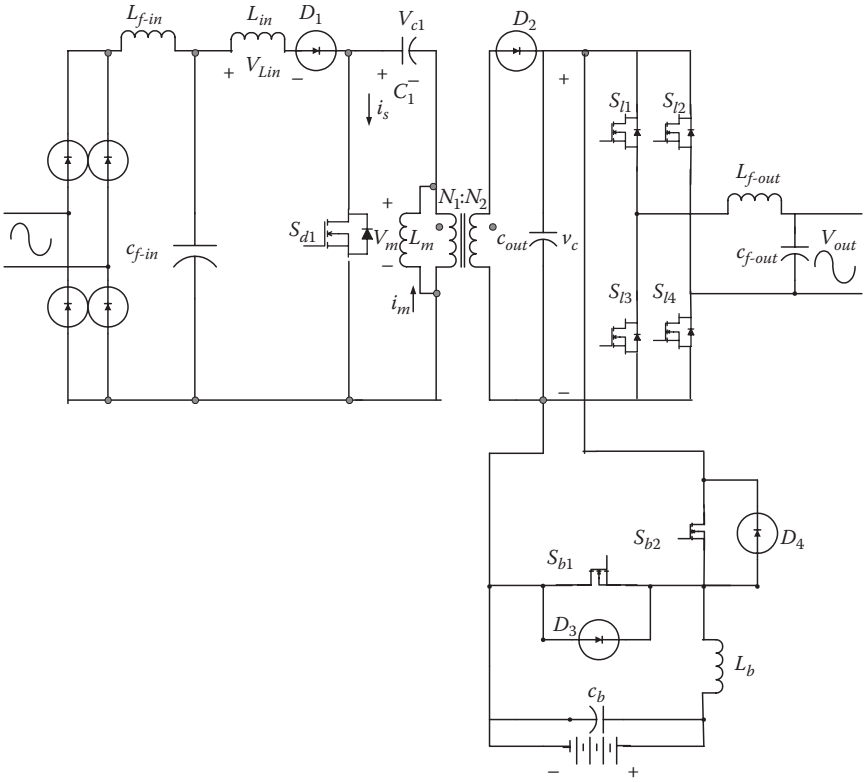


Figure 14.3 Configuration of proposed on-line UPS system based on BIFRED converter.

BIFRED features voltage source function for both the following inverter and bi-directional DC/DC converter (Figure 14.3).

The DC/AC inverter consists of a DC-link bus capacitor C_{out}, switches S_{l1} to S_{l4}, and an output LC filter. It operates in a high-frequency pulse width modulation (PWM) pattern in order to provide high-quality sinusoidal output voltage. The charger/discharger is, in fact, a bi-directional DC/DC converter and consists of switches S_{b1} and S_{b2} as well as a DC inductor L_b.

The switch S_{b2} chops the high DC-link voltage V_{dc} and steps it down to low battery voltage V_{bat} during normal operation mode and charges the battery bank. In this way, it eliminates the problems associated with the high battery voltage, such as space, cost, reliability, and safety issues.

During the energy-stored mode of operation the boost converter steps up the low battery voltage V_{bat} to high DC-link voltage for proper operation of the back-end inverter.

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In the following paragraphs, we introduce the operation modes for the converters.

14.1.1 Normal Operating Mode

The BIFRED converter has five modes of operation. A comprehensive study of the operating principles of the BIFRED converter was presented earlier. DCM-DCM is the desired mode. The control strategy applied keeps the converter in this mode of operation. The boost converter shapes the input current and the flyback converter provides the system isolation and the output voltage regulation. The conducted EMI in the converter is reduced by an input EMI filter. The capacitor C_1 reduces the output voltage ripple for the BIFRED converter and, at the same time, provides a wide bandwidth to improve the shape of the input current. Figure 14.4 shows the current waveform of the BIFRED converter in the desired mode.

When switch Sd1 is on, the circuit has the configuration shown in Figure 14.5. When switch is off, the circuits in the first stage, in the second stage, and in the third stage are shown in Figures 14.6, 14.7, and 14.8, respectively.

The full-bridge inverter consists of a DC capacitor and four switches (IGBTs) S_{l1}, S_{l2}, S_{l3}, and S_{l4} connected in series two by two in two inverter legs. By turning on and off the switches, the voltage applied across the load can be +Vdc, –Vdc, or 0. When switches S_{l1} and S_{l2} are on, switches S_{l3} and S_{l4} are off and the load voltage is +Vdc. When switches S_{l4} and S_{l4} are on, switches S_{l1} and S_{l2} are off and the load voltage is –Vdc. In addition, when switches S_{l1} and S_{l3} are on, switches S_{l2} and S_{l4} are off and the load voltage is 0. Similarly, when switches S_{l2} and S_{l4} are on, switches S_{l1} and S_{l3} are off and, accordingly, the load voltage is 0. In order to avoid

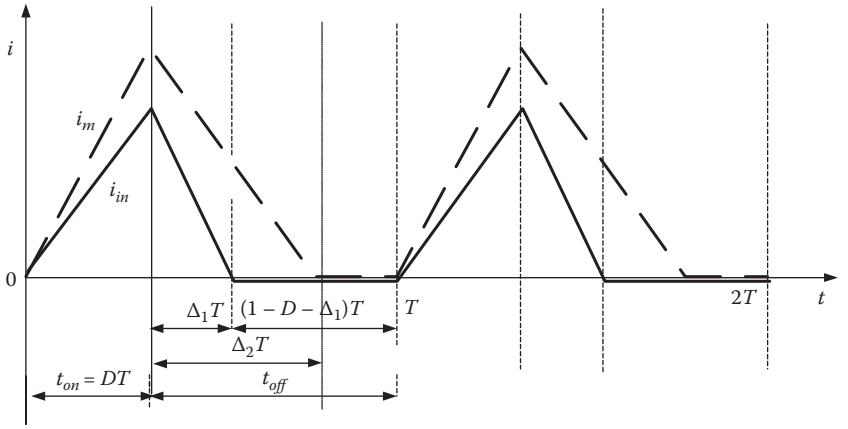


Figure 14.4 Current waveform of BIFRED converter in desired mode.

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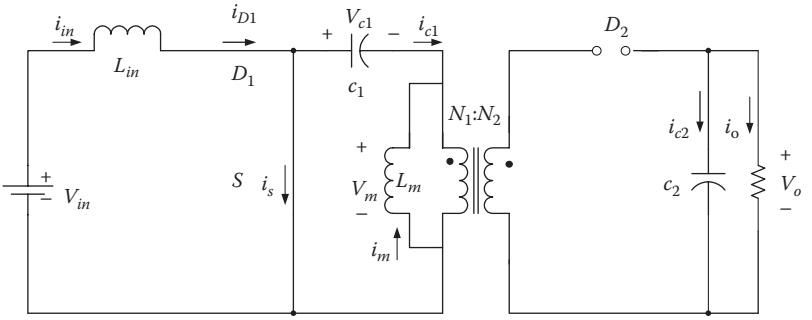


Figure 14.5 Isolated BIFRED converter (during DT, switch: on).

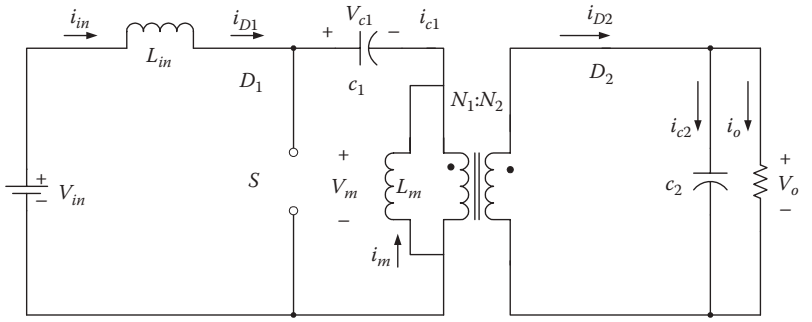


Figure 14.6 Isolated BIFRED converter (during DT, switch: off).

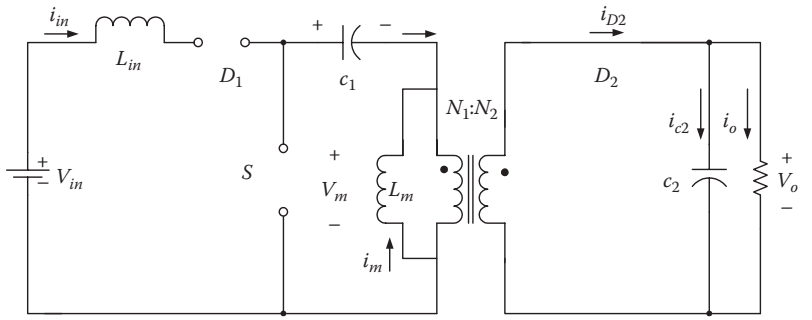


Figure 14.7 Isolated BIFRED converter during $(1 - D - \Delta_1)\,T$, $\Delta_1 < \Delta_2$, switch: off.

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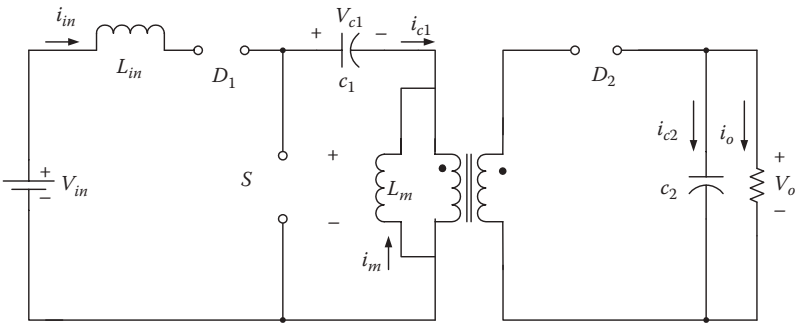


Figure 14.8 Isolated BIFRED converter (during $(1 - D - \Delta_2)\ T$, $\Delta_1 < \Delta_2$, switch: off).

shoot-through faults, there is always a dead-band between the time when one of the switches in an inverter leg is turned off and the other is turned on.

In the PWM switching schemes, the output voltage is directly proportional to the duty cycle of the switches and the amplitude of the DC bus voltage Vdc. The output voltage can range from –Vdc to +Vdc. Since the amplitude of the input DC voltage is usually fixed, the only way to shape the output voltage is to control the duty cycle of the switches. In order to do so, in the case of PWM technique, a sinusoidal reference signal oscillating at the desired frequency is compared with a high-frequency triangular carrier waveform. The frequency of the triangular carrier waveform determines the inverter switching frequency and is kept constant at 20 kHz.

In the unipolar PWM switching scheme used for driving the back-end inverter, the output voltage is either switched from high to zero or from low to zero, unlike in the bipolar switching scheme, where the switching takes place directly between high and low. As a result, the content of high-order harmonics in the output voltage is much lower compared to the corresponding one from the bipolar switching scheme. Consequently, the required output filter can be considerably smaller and the overall efficiency of the system is higher.

The control strategy employs two control loops: one outer voltage loop and one inner current loop. The outer control loop uses the output voltage as a feedback signal, which is compared with a reference signal. A PI integrator to achieve stable output voltage under steady-state operation compensates the error. This error is also used as a reference signal for the inner current regulator loop, which uses the output current as a feedback signal. The minor current loop is much faster than the outer voltage loop and improves the dynamic response of the inverter. As a result, the output voltage is of very high quality even with highly nonlinear loads. The switching frequency is 20 kHz.

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14.1.2 Battery Charge Regulation Mode

The bi-directional DC/DC topology is a combination of a buck converter and a boost converter. In the battery charge regulation mode, switch S_{b1} and diode D_4 are off. Capacitor C_{out}, switch S_{b2}, inductor L_b, diode D_3, capacitor C_b, and battery consist of a buck converter. The battery is in the charge mode. Figure 14.9 shows the circuit of the battery charge regulation mode.

14.1.3 Backup Mode

In the backup mode of operation, when the input AC voltage is out of the permissible tolerance range or is not available at all, switch S_{b2} and diode D_3 are off. The boost converter consists of capacitor C_{out}, switch S_{b1}, inductor L_b, diode D_4, capacitor $C_{b,}$ and battery. The battery supplies all the power to the load. Figure 14.10 shows the circuit for the backup mode.

14.1.4 Control Strategy

The small signal output voltage to duty cycle transfers function of the BIFRED converter derived from the state space averaging method shows one pole for this kind of converter topology. Therefore, simple control can be achieved according to the voltage follower approach. Though this method can cause a pulsating triangle waveform in the input inductor current, the near unity power factor can still be implemented. Figure 14.11 shows this kind of control strategy for different modes.

In the normal mode of operation, switch S_1 will be off, and switch S_2 needs to connect to pin a. In the battery charge regulation mode, switch S_1 will be on and switch S_2 also needs to connect to a pin, too. In the backup

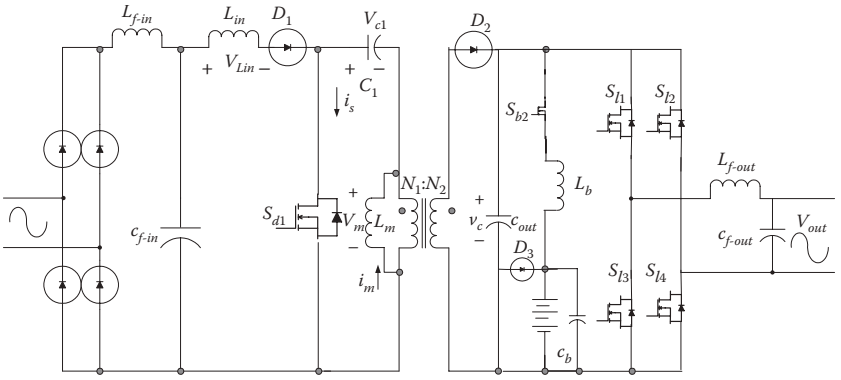


Figure 14.9 Circuit for battery charge regulation mode.

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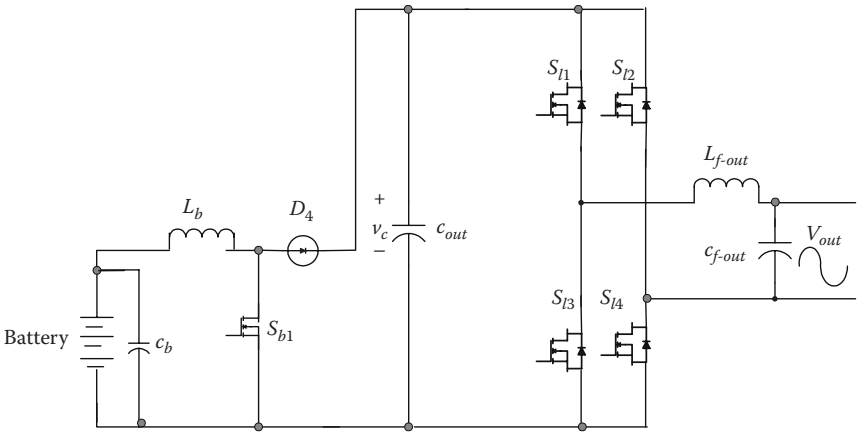


Figure 14.10 Circuit for backup mode.

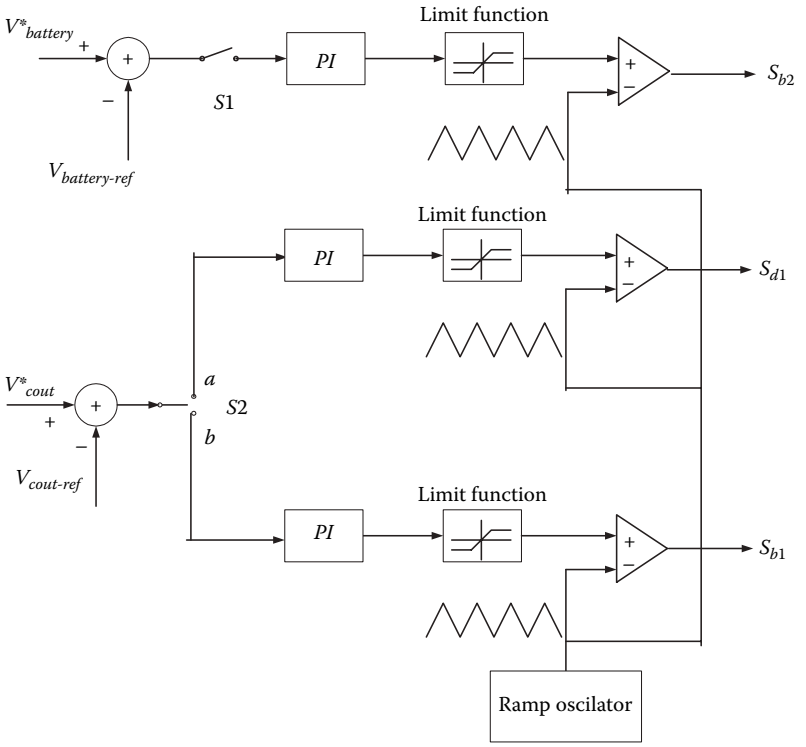


Figure 14.11 AC/DC-DC/DC converter control block diagram.

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mode, switch S_1 will be off, and switch S_2 needs to connect with pin b. For the PWM-VSI control, the SPWM control method is employed to regulate the output AC voltage. Figure 14.12 shows this kind of control strategy.

14.2 Integrated Switched-Mode Power Converters for Switched Reluctance Motor Drives

The simpler mode for the integrated converter for switched reluctance motor (SRM) drives is shown in Figure 14.13, where converter set 1 owns the PFC preregulator function. Converter set 2 owns the DC/DC conversion function. Converter set 3 owns the DC SRM drive function as shown in Figure 14.14.

For converter sets 1 and 2, a traditional method is to use a PFC preregulator followed by a DC/DC stage. However, the output voltage from the preregularor has a considerable ripple at twice the line frequency, which does not allow a fast output voltage regulation of the PFC. The compensation of this voltage ripple would make the input line current distort; therefore, the voltage loop must have a lower bandwidth than the line frequency. In order to improve the performance of converter set 1 with the PFC preregulator function and converter set 2 with the DC/DC converter function, single-

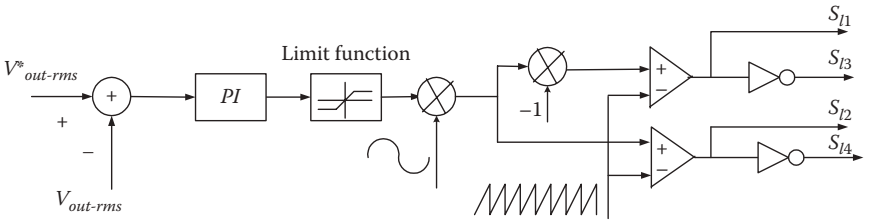


Figure 14.12 DC/AC inverter control block diagram.

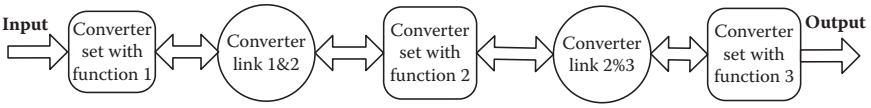


Figure 14.13 Integrated converter with general model for SRM drives.

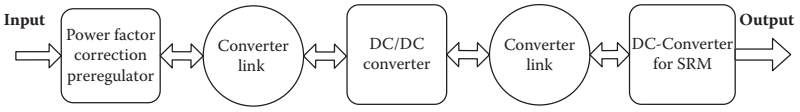


Figure 14.14 Integrated converter for SRM drives.

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stage topologies are used to form the sub-integrated converter shown in Figure 14.15, where single-stage converters for medium-power PFC and fast output voltage regulation can be insulated boost, Ćuk, SEPIC, and resonant converters as well as parallel power factor correction [8]–[14].

As shown in Figure 14.16, there are three kinds of converter link models for the basic SRM drives. Most of them can be linked by method 3. Methods 1 and 2 are suitable for the variable DC-link voltage converter, asymmetric half-bridge converter, and bifilar converters. For methods 1 and 2, the extra capacitor is smaller than the main DC-link capacitor so that the voltage across it rises more quickly and to a higher voltage. Faster commutation and turn-on are achieved. The next time the phase is energized, current rises more quickly in the winding as a result of the boost voltage. For the link with method 1, converters are not suitable for the generation mode of operation. However, for method 2, converters are suitable for generator applications.

As an example, the variable DC-link voltage converters for SRM drives are discussed. A converter for SRM with variable DC link voltage

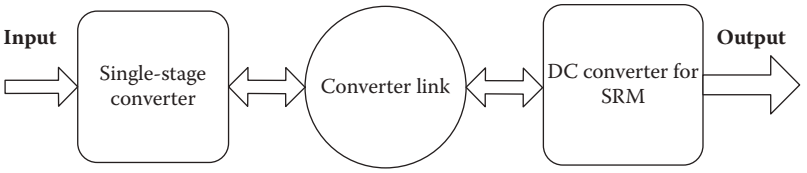


Figure 14.15 Integrated converter with sub-integrated converter for SRM drives.

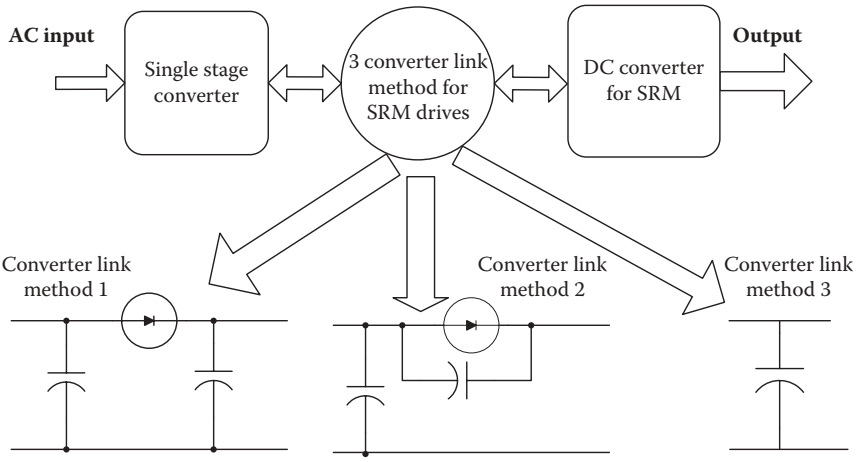


Figure 14.16 Converter link with different methods for SRM drives.

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is shown in Figure 14.17, where capacitor C_1 is the converter link with method 1.

In order to improve the system efficiency and reduce the cost, we can integrate a single-stage converter with the DC/DC converter by different methods. Based on the analysis shown in Figures 14.18, 14.19, and 14.20, we can clearly see the proposed integrated converters for variable DC-link converters in Figures 14.21, 14.22, and 14.23.

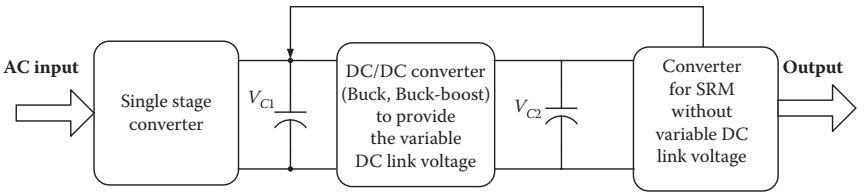


Figure 14.17 Converter for SRM decomposed into two parts: DC/DC converter for variable DC-link voltage and converter for SRM without variable DC-link voltage.

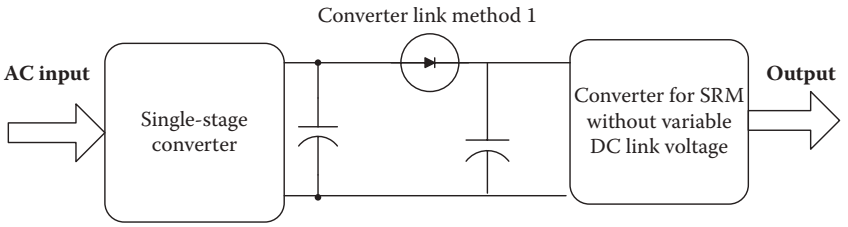


Figure 14.18 Integrated converter for SRM drives with converter link method 1.

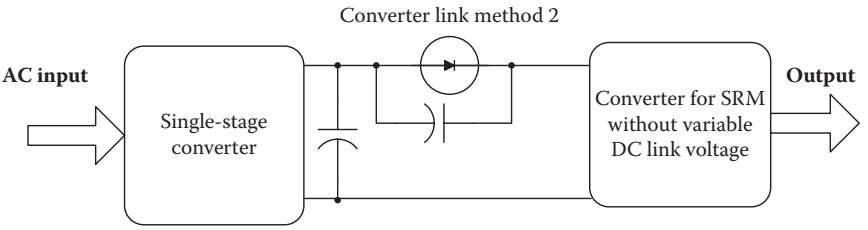


Figure 14.19 Integrated converter for SRM drives with converter link method 2.

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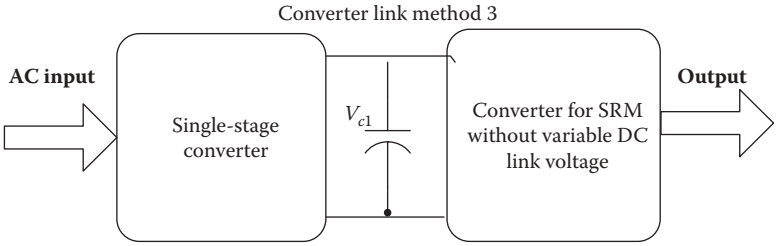


Figure 14.20 Integrated converter for SRM drives with converter link method 3.

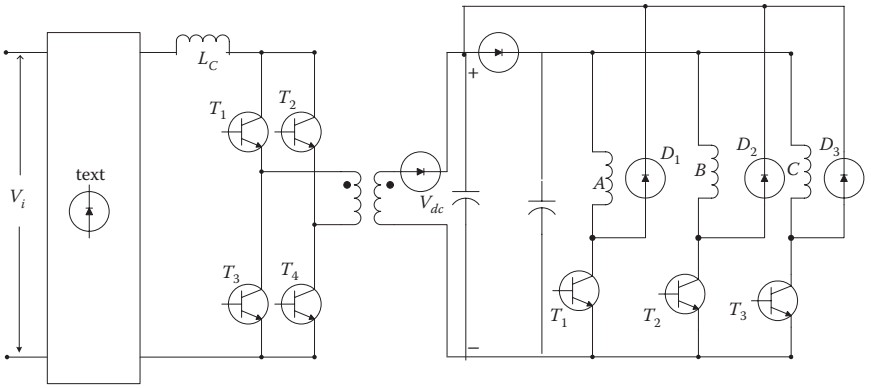


Figure 14.21 Proposed integrated converter for SRM drives with converter link method 1.

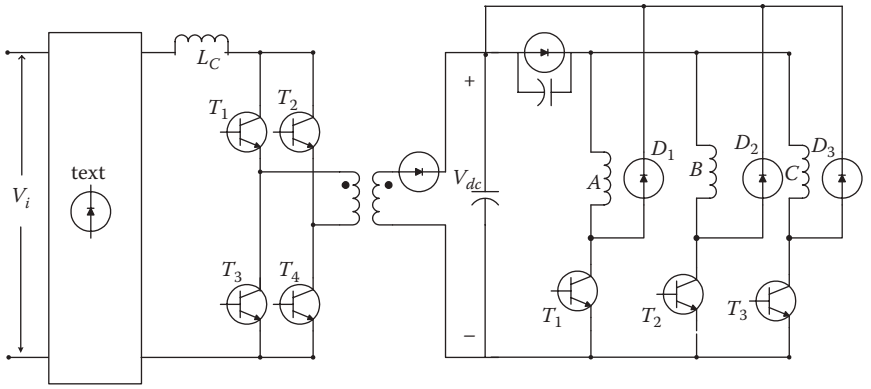


Figure 14.22 Proposed integrated converter for SRM drives with converter link method 2.

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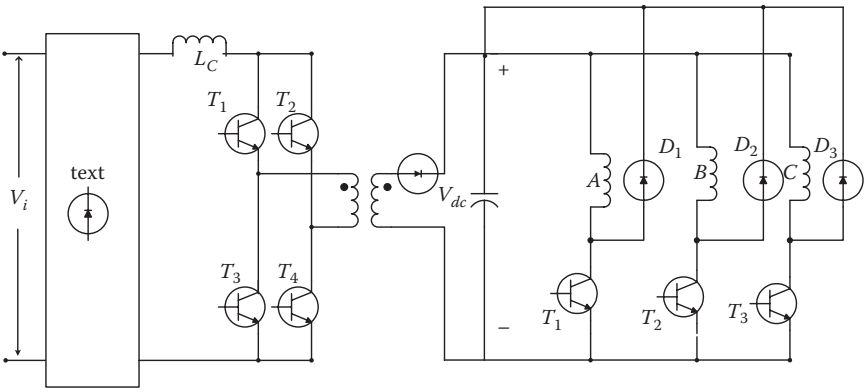


Figure 14.23 Proposed integrated converter for SRM drives with converter link method 3.

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chapter fifteen

Review of Digital Control Techniques in Power Electronics

Conventionally, power electronics converters and motor drives have been controlled using analog integrated circuit technology and linear system design techniques. Analog control techniques have been predominant due to their simplicity as well as their low implementation cost. However, they are sensitive to environmental disturbances such as noise, temperature, and aging. Besides, implementation of sophisticated advanced control techniques employing analog circuits is inherently difficult. In this chapter, a comprehensive review of digital controllers for power converters and motor drives is presented.

15.1 Advantages of Digital Control

Over the last two decades, digital control methods and digital controllers have become pervasive in applications such as motor drives and three-phase power converters for utility interfaces. Digital control provides many advantages over analog control. Merits of digital control can be studied under integration and performance categories [1].

15.1.1 Integration

The digital controller is an HDL-based digital very large scale integration (VLSI) design, which implies a reduced number of components and weight, shorter development time, and the flexibility to target the realization to different implementation technologies [1]–[3]. As a result, the digital controller technology can benefit from size, speed, and cost scaling in sub-micron complementary metal oxide semiconductor (CMOS) digital technologies. Another important aspect of enhanced integration capabilities is intelligent, adaptive power management techniques where the supply voltage is dynamically adjusted to minimize the total power consumption.

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15.1.2 Performance

Digital controller technology has the potential to offer a number of performance enhancements in power electronics applications. Some of them are as follows:

- Digital components are less susceptible to aging and environment variations [1]–[7].
- They are less sensitive to noise [4].
- The fact that digital control systems are programmable gives the flexibility that changing a controller does not require an alteration in the hardware [4], [5].
- They provide less sensitivity to parameter variations [4].
- Significant power savings can be obtained using adaptive power management schemes that benefit from system integration based on digital controller technology [1].
- The complexity of the digital control system is contained mostly in software [7].
- Digital controller technology opens the possibility of implementing more advanced control concepts, such as adaptive control and predictive digital current mode control, which would be considered impractical with standard analog circuits [1], [8].
- Electromagnetic interference levels (EMIs) are reduced [6], [9].
- The circuit configuration of the board is very simple, surface-mounted parts for tuning are unnecessary, and all control variables and parameters can be adjusted automatically [10].

Clear technical advantages of digital control, combined with the tremendous growth of processing power of digital VLSI devices at ever-decreasing costs, resulted in widespread adoption of digital control technology in power electronics applications.

15.2 Disadvantages of Digital Control and New Trends

Even though some advantageous can be obtained using digital control systems, there are some issues that should be carefully considered when using these converters. Some of these issues are as follows.

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15.2.1 Limited Analog-to-Digital Conversion Resolution and Range

Depending on the number of bits used in the digital signal processor (DSP) or micro-controller, numerical values corresponding to the measured signals in the digital system are restricted to a finite number of discrete values. For instance, an 8-bit analog to digital converter has 255 discrete levels. Therefore, it can only measure a voltage to one part in 255 of its reference voltage. So, for a typical reference voltage of 5 V, the voltage converted to a digital representation is quantized into steps of 5/255 or 19.61 mV. Loss of resolution results in increasing steady-state error and limit cycles. Moreover, an additional circuitry is required to convert the real output voltage to a compatible level with the analog-to-digital converter (ADC) [7].

15.2.2 Limited Digital PWM Resolution

One problem with the microprocessor-based high-frequency PWM converters is resolution limitation caused by hardware timers [11]. For instance, if the minimum timing cycle is 10 μs with the frequency of 16 MHz, and PWM switching frequency is 0.2 MHz, the resolution of DC PWM is 1 in 50, since the period is 500 μs, and the amplitude modulating resolution of synchronized pulse-width modulation (SPWM) is not better than 1 in 25. Generally, the digital control PWM has the following problems [11]:

1. The output voltage accuracy of DC PWM is finite.
2. The amplitude modulating resolution of SPWM is also limited.
3. The THD of SPWM is higher than natural sampled PWM.

Therefore, in the design of a digital controller, to achieve stable operation, the limit of digital pulse width modulation should be considered. References [11] and [12] present different approaches to solve this issue.

In reference [11], *double PWM* is introduced to improve digital PWM (DPWM) resolution. This method chooses high-frequency switching along with low-frequency modulating. It adds a lower frequency PWM to the conventional PWM. The fundamental PWM frequency is switching frequency and the second-order PWM determines the modulation frequency. The ratio of the switching frequency to the modulation frequency is called modulus (n). The double PWM operating process is shown in Figure 15.1, where n = 4. The average duty ratios of Figures 15.1(c-1) and (c-2) are

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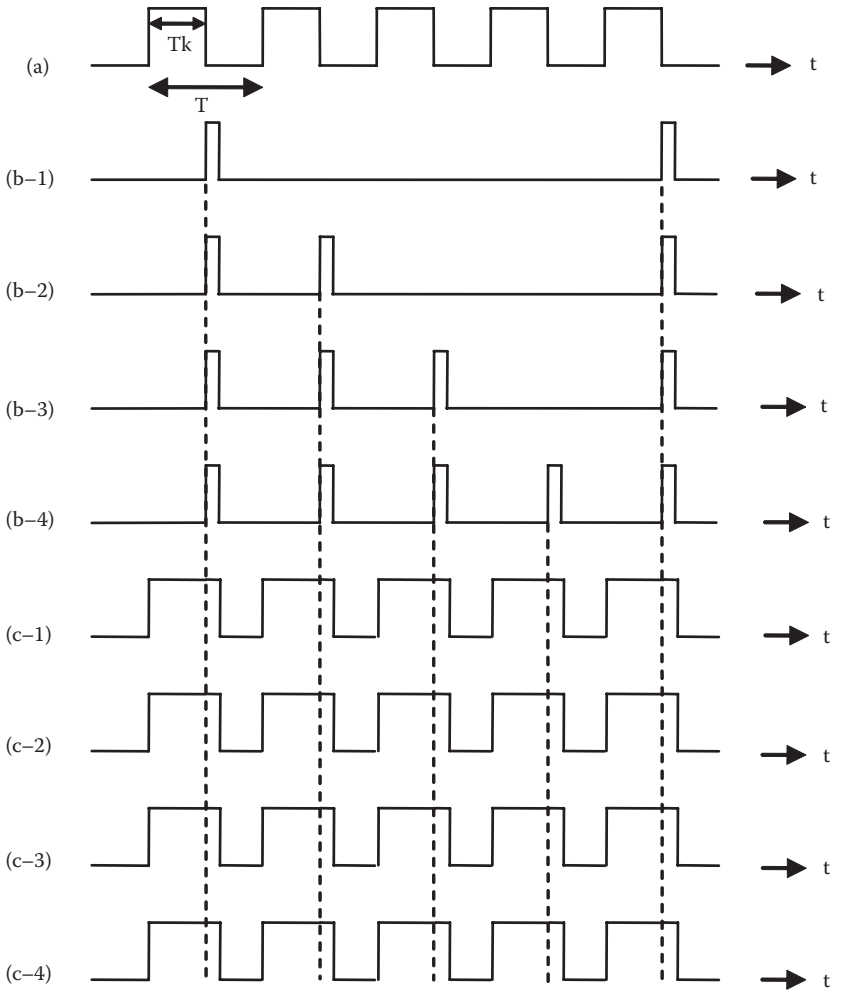


Figure 15.1 Double PWM operation process. (a) Conventional PWM, (b1–4) second-order PWM, (c1–4) double PWM.

$$D = \frac{T_k}{T} + \frac{T_b}{4T}$$

and

$$D = \frac{T_k}{T} + \frac{T_b}{2T}$$

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respectively. The duty ratio of minimum average pulse ratio is

$$D_{\min} = \frac{T_b}{nT}.$$

The minimum average pulse width reduces n times and the resolution increases. Double PWM includes the advantage of low- and high-frequency power conversion and avoids their respective shortages at the same time.

15.2.3 Steady-State Oscillations (Limit Cycles)

Another problem with digitally controlled systems is limit cycles [2], [4], [12]. defined as steady-state oscillations of output voltage and other system variables at frequencies lower than the converter switching frequency. Limit cycles may result from the presence of signal amplitude quantizers like the ADC and DPWM modules in the feedback loop. Steady-state limit cycling may be undesirable if it leads to large, unpredicted output voltage variations. Moreover, since the limit cycle amplitude and frequency are hard to predict, it is difficult to analyze and compensate for the resulting output voltage noise and the electromagnetic interference (EMI) produced by the converter. Limit cycles generate if DPWM tries to regulate the output voltage into a desired level for which there is no close ADC level. In this situation ADC distinguishes this as a steady-state error and forces the DPWM to change the discrete duty ratio to fix the problem. Once this happens the DPWM will not provide the desired output voltage, and therefore, because of the sequential interaction between the ADC and DPWM, some unwanted steady-state oscillations will be generated. Limit cycles and their elimination methods have been comprehensively studied by Peterchev and Sanders [12].

15.2.4 Inherent Time Delay

Due to the time delay required for analog-to-digital conversion, computation of the control algorithm by the processor and PWM generation calculated input of the system will be used at the next cycle [4]. In other words, there is one switching period time delay in the control loop of digital systems. This delay can be modeled by the function e^{-Ts}, where T is the sampling period of the digital controller. As a result of delay, the phase margin decreases and the control loop bandwidth should be sacrificed to gain stability. Bandwidth reduction degrades the transient response of the system. Sprock and Ping [13] present predictive schemes to compensate the

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inherent time delay of the system. Predictive control tries to compensate the time delay of the system by updating the controller using estimated value of output voltage at $(k+1)T$ in the k^{th} interval.

15.3 Structure of Digital Controllers

Figure 15.2 shows the block diagram of a typical digital control system [14]. A digital system operates on samples of the sensed plant output. The analog-to-digital converter (A/D) converts the sensed output voltage to a digital number, which is readable by a digital controller. The digital controller generates the input of the system, which in the case of a converter is the duty cycle (d), based on the processed data. The input and output of a digital controller are related by a linear difference equation such as

$$\sum_{i=0}^{n} \alpha_i u\left(k-i\right)T = \sum_{j=0}^{m} b_j e\left(\left(k-j\right)T\right) \tag{15.1}$$

where $e(kT) = V_{ref} - v_{out}(kT)$.

15.4 Digital Design

The design of a digital control system is the process of choosing the difference equation or equivalent z-domain transfer function for the controller, which will yield an acceptable performance for the closed-loop system. The performance specifications can take on many different parameters, such as rise time, settling time, percent overshoot, close-loop frequency response magnitude, bandwidth, and damping ratio.

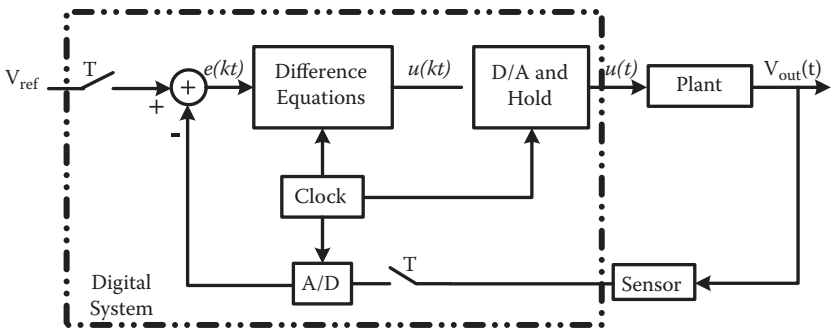


Figure 15.2 Typical digital control system block diagram.

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In the design of digital compensators, two approaches are generally applied [4], [5]. The first is to ignore any zero-order holds (ZOHs) and samplers in the control loop and prepare a preliminary design in the s-domain. The design should then convert to a discrete time by some approximate technique to have a discrete-time compensator. The second method is to convert the continuous time plant with zero-order hold or first-order hold or any other method and samplers to a discrete plant using some approximate technique. Once a discrete-time approximation of the plant is available, then the discrete-time compensator can be designed directly in the z-domain using methods similar to the continuous time frequency response methods or root locus or other methods.

15.4.1 Digital via Emulation

The first method, which is designing the controller in continuous time domain and then converting it to an equivalent digital controller, is called digital redesign approach or digital design via emulation. This method has an advantage to direct digital design in that engineers are more used to thinking clearly in the s-plane than the z-plane. It has a disadvantage since in the process of conversion to a discrete-time compensator, the z-plane poles are distorted from where they are needed, and hence a trial-and-error design procedure may be required. There are several transformation techniques to convert a continuous controller to the digital equivalent one, which can yield results of different performance [4], [14], [15]. These techniques are shown in Table 15.1.

15.4.2 Direct Digital Approach

The second method, which is directly designing the digital controller, is called direct digital approach. The digital controller is designed in the discrete-time domain using the step invariant model of a continuous time plant when zero-order hold is used. Once a discrete time approximation of the plant is available, the controller is designed directly in the z-domain using methods such as discrete time frequency response method, root locus method, deadbeat method, or other methods [15].

This method has the advantage that the poles and zeros of the discrete compensator are located directly, and the designer can pick these locations a priori. A disadvantage is that it is difficult for the designer to visualize exactly where the z-domain poles and zeros need to be located to satisfy system performance [4], unless pole/zero-matched techniques are used to locate their place in the z-domain, which in turn may cause some distortion.

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Table 15.1 Discretization Methods

Transformation method	s-Domain	z-Domain
Forward	s	$\frac{z-1}{T_s}$
Backward	s	$\frac{1-z^{-1}}{T_s}$
Bilinear (Tustin)	s	$\frac{21-z^{-1}}{T_s 1+z^{-1}}$
Prewarp	s	$\frac{w}{\tan(wT/2)}\frac{z^{-1}}{z+1}$
Step invariant	$G_c(s)$	$Z\ \frac{1-e^{-T_s s}}{s}G_c(s)$
Pole/zero match	$\frac{s+a}{s+a\pm jb}$	$\frac{1-z^{-1}e^{-aT_s}}{1-2z^{-1}e^{-aT_s}\cos bT_s+z^{-2}e^{-2aT_s}}$
Matched pole/zero	e^{sT}	z

15.4.3 Root Locus Approach

The root locus [14]–[17] is a graphical method that solves an n^{th}-order polynomial. By adjusting the controller parameters, the poles and zeros of the system can be tuned to favorable positions. The tuning process, however, can be long, especially if there are a number of undecided controller parameters [15].

15.4.4 Bode Plot or Frequency Response Approach

The frequency response method [14], [16], [17] is particularly convenient to practicing engineers who are familiar with the Bode plot design method in the s-domain, and can use the same concept such as the gain crossover frequency and gain/phase margins. The limitation of this technique, however, is that the sampling frequency must be at least 10 times higher than the closed-loop bandwidth [15].

15.4.5 Deadbeat Control

Another way to optimize digital control performance is to use the deadbeat concept, where the control variable is calculated ahead of time and

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in such a way that the error is canceled out after a fixed number of steps [14]. Typically, this technique relies on the model of the process, which also makes it sensitive to model uncertainties. In addition, deadbeat algorithms can be computationally intensive and thus require extensive processor resources. Nevertheless, deadbeat control offers a much faster dynamic response than conventional control and can be successfully applied to switching circuits. The deadbeat control is highly dependent on the accuracy of the plant function. Therefore, the advantage of the deadbeat controller is not obvious in most cases [15]. Assume that the plant is described by equation (15.2) and the overall closed loop system is presented by equation (15.3).

$$G(z) = \frac{B(z)}{1 + A(z)} \tag{15.2}$$

$$H(z) = \frac{Y}{R} = \frac{DG}{1 + DG} \tag{15.3}$$

where *D(z)* is the digital controller for the discrete system, based on equation (15.3) *D(z)* can be presented as equation (15.4):

$$D = \frac{1}{G}\frac{\frac{Y}{R}}{1 - \frac{Y}{R}} \tag{15.4}$$

The deadbeat controller, which forces the output of the closed-loop system to a predefined value, such as $y(m)$, after m sampling period is as follows [18]:

$$D(z) = \frac{q_0(1 + A(z))}{1 - P(z)} \tag{15.5}$$

where

$$q_0 = 1 \Big/ \sum_{i=1}^{n} b_i, \quad B(z) = \sum_{i=1}^{n} b_i z^{-i}, \quad A(z) = \sum_{i=1}^{n} a_i z^{-i},$$

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$$a_0 = 1,$$

and

$$\frac{Y}{R} = \sum_{i=1}^{m} p_i z^{-i} = P(z).$$

The authors of Reference 19 proposed a digital controller based on the predictive deadbeat control approach, which updates the duty ratio of the PFC switch only once in several periods. This is to account for the fact that the PFC converter is switching so fast that the DSP does not have enough time to complete other power stages and perform other tasks. In Reference 20, the same control method for the digital operation of a buck converter working in the CCM has been applied. The proposed controller is similar to the two-loop current mode control.

Deadbeat control can also be implemented in UPS systems to synthesize the sinusoidal output voltage waveform as well as to minimize the THD in the output voltage signal. In Reference 21, a deadbeat control algorithm is developed to control the duty cycle such that the output voltage tracks the sinusoidal reference voltage at each sampling instant. This method has very fast response to load disturbances and nonlinear loads. Yet the drawbacks of the proposed method are (a) at each sampling instant, both output voltage and capacitor current measurements are required, and (b) the feedback gains must be adjusted manually by trial and error since the theoretical converter parameters determined from the measured L, C, and R are not the true values due to the nonlinear effects. To overcome these drawbacks, the authors of Reference 22 proposed a deadbeat control scheme using only a voltage sensor. The controller uses voltage signals at present and previous sampling instants, i.e., the pulse width signal from the previous sampling interval and the reference signal for the next sampling interval. The proposed method, which is called output feedback one sampling ahead preview control, enjoys the following advantages: (a) low THD, (b) very fast transient response, (c) stable operation for various load conditions, and (d) applicability to three-phase systems [23], [24].

A disadvantage of the proposed methods is that the maximum available pulse is limited by the computation delay time of the microprocessor. The maximum pulse width is less than one sampling interval. Hence, the maximum amplitude of the output voltage is limited to the DC supply voltage. Moreover, this limitation may result in saturation of the controlled pulse width, distortion of output voltage, and instability. To overcome these problems, a modified deadbeat control law based on the sampled-data modeling of the PWM inverter system is proposed in

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Reference 25 to expand the pulse width to the entire sampling interval. In this method, two kinds of pulse patterns are used to increase the duty ratio of the pulses, considering the effect of computation time. The authors of Reference 26 proposed a modified one sampling ahead preview (OSAP) control approach to increase the maximum pulse width. In this approach, the pulse width in the k^{th} sampling interval is computed by using the output voltage sampled at the previous sampling instant *k-1.* Hence, the pulse width determination can be completed during the previous interval and the pulse width can be extended to the theoretically maximum limit, which is the sampling interval *T.* Deadbeat control has also been employed in current mode control for the active filters [27]-[29].

In deadbeat control, as mentioned earlier, any nonzero vector is driven to zero in at most *m* sampling periods if the magnitude of the scalar is unbounded. The settling time depends on the sampling period since the response is deadbeat at most *m* sampling periods. The control signal must have an extremely large magnitude to achieve a very small settling time. The designers must pay attention to the upper bound of the actual control force so that the deadbeat effect can be guaranteed. If the magnitude is increased sufficiently, a saturation phenomenon always happens [30]. If saturation occurs in the magnitude of the control signal, the response can no longer be deadbeat and the settling time will be more than *n* sampling periods.

15.4.6 Raggazini's Controller Design Method

Direct design method of Raggazini is an alternative design method, which has been found to be useful in adaptive controls [14]. Suppose we are given a discrete transfer function *G(z)* of the plant and a desired closed loop transfer function *H(z).* The structure is assumed to be a unity feedback system and the design is to choose the controller transfer function *D(z)* to realize *H(z).* The overall transfer function is given by

$$H(z) = \frac{DG}{1 + DG} \tag{15.6}$$

from which we get the direct design formula

$$D(z) = \frac{1}{G(z)} \frac{H(z)}{1 - H(z)} \tag{15.7}$$

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From the above equation we see that this design calls for a *D(z)*, which will cancel the plant effects and add whatever is necessary to give the desired result.

In Raggazini's direct method, first of all, the design should be *causal*. That means *H(z)* must have a zero at infinity of the same order as the zero of *G(z)* at infinity. Second, since *D(z)* is not to cancel a zero of *G(z)*, *1-H(z)* should contain as zeros all the poles of *G(z)* that are outside the unit circle. Likewise, since *D(z)* is not to cancel a zero of *G(z)*, *H(z)* should contain all the zeros of *G(z)* that are outside the unit circle.

Finally, considering the constraint of steady-state accuracy, if the system is to be type 1 [14], [16], [17] with velocity constant K_v, we must have zero steady-state error to a step and $1/K_v$ error to a unit ramp, which means

$$-T\left.\frac{dH}{dz}\right|_{z=1} = \frac{1}{K_v} \tag{15.8}$$

Therefore, to realize a closed-loop transfer function limited by causality and stability constraints, the direct design method of Raggazini gives an appropriate *D(z)*.

15.4.7 State-Space Design

State-space description of a discrete system is given by

$$\begin{aligned} x(k+1) &= \Phi x(k) + \Gamma u(k) \\ y(k) &= \mathrm{H}x(k) + Ju(k) \end{aligned} \tag{15.9}$$

State-space design methods consist of two independent steps. The first step assumes that we have all the state elements at our disposal for feedback purposes. In general, this is not a good assumption. It merely allows the designer to proceed with the first design step, namely, the control law. The second step is to design an *estimator* or *observer*, which estimates the entire state vector. The final control algorithm consists of a combination of the control law and the estimator with the control law calculations based on the estimated states rather than on the actual states.

15.4.7.1 State Feedback Design (Control Law Design)

The control law is the feedback of a linear combination of all the state elements, which is

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$$u = -\mathbf{K}x = -\begin{bmatrix} K_1 & K_2 & \cdots \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \\ \vdots \end{bmatrix} \tag{15.10}$$

The z-transform of substituting equation (15.10) in equation (15.9) yields

$$(z\mathbf{I} - \Phi + \Gamma\mathbf{K})\mathbf{X}(z) = 0 \tag{15.11}$$

The control law design, then, consists of finding the elements of $\mathbf{K}$ so that the roots of the characteristic equation of the system, equation (15.12), which are the poles of a closed-loop system, are in the desired locations.

$$\left|z\mathbf{I} - \Phi + \Gamma\mathbf{K}\right| = 0 \tag{15.12}$$

Given desired pole locations at $z_i = \beta_1, \beta_2, ..., \beta_n$. , the desired control characteristic equation is

$$\alpha_c(z) = (z - \beta_1)(z - \beta_2)...(z - \beta_n) = 0 \tag{15.13}$$

Required elements can be obtained by matching the coefficients of powers of z in equations (15.12) and (15.13), in which there are n equations for an nth-order system.

15.4.7.2 State Estimator Design (Estimator Design)

The control law designed above assumed that all state elements were available for feedback. Typically, not all elements are measured; therefore, the missing portion of the state needs to be reconstructed for use in the control law. There are two basic kinds of estimates of the state: *x(k).* The first one is called *current* estimate; $\hat{x}$ *(k),* which is based on measurement of up to *y*(*k*) including the *k*th instant. The second one is called *predictor* estimate, $\hat{x}$ *(k),* which is based on measurements up to *y(k-1).* The idea eventually will be to let $u = -\mathrm{K}\,\hat{x}$ or $u = -\mathrm{K}\,\bar{x}$, replacing the true state used in equation (15.10) by its estimate. Detailed state-space design methods for discrete time systems are presented in Reference 4.

The simulation and experimental results of the applying three controller design approaches to a forward converter are presented in Reference 31. First, a controller is designed in continuous domain and then it is converted to discrete domain using bilinear transformation. Second, the converter is controlled using a proportional integral derivative (PID) controller in discrete domain. Finally, deadbeat control is applied to the converter.

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Simulation and experimental results of applying these three methods to the forward converter show that the deadbeat controller has the largest bandwidth as well as smallest maximum recovery time, while the PID controller has the highest gain at 10 Hz as well as the largest phase margin. The results of Reference 31 show that due to the creation of additional phase shift in the discretized analog controller, its stability is not as good as others. The digital PID has the best performance among these three. For the deadbeat controller, the output error is forced to zero within two sampling periods. This implies a large magnitude of duty cycle. Since the range of duty cycle is limited, the requirement is not satisfied. Therefore, the advantage of deadbeat controller is not clear.

The authors of Reference 32 used design via emulation method to design a digital PID controller for a buck converter. Backward method was used to convert the controller into z-domain. One approach, which utilizes two sets of controller gains, is suggested to improve the steady-state response and maintain the transient response. Applying this method yields either a system with a faster transient response but a higher steady-state output voltage ripple, or a system with a slower transient response but a better steady-state output voltage ripple, depending on the controller parameters. The decision to select one of these two designs can be based on overall closed-loop requirements.

The authors of References 33 and 34 have applied improved versions of the prewarp transformation method to an existing continuous system to convert it to its discrete equivalent system. These two methods are compared in Reference 35.

15.5 Digital Control Techniques

In this section some techniques that commonly apply to digital control systems are presented.

15.5.1 Digital Current Mode Control

Digital current mode control is a new method for improving the dynamic characteristics of high frequency PWM converters. It is an approach in which a digital processor carries out the whole control strategy in software. It is also a true current mode control, which compares samples of the average inductor current over each switching cycle to the current program level. These two features make it a very powerful technique. Figure 15.3 shows the block diagram of an average current mode control scheme applied to a simple buck converter. This type of control is similar to the digital current mode control method, so it is useful to briefly examine its operation.

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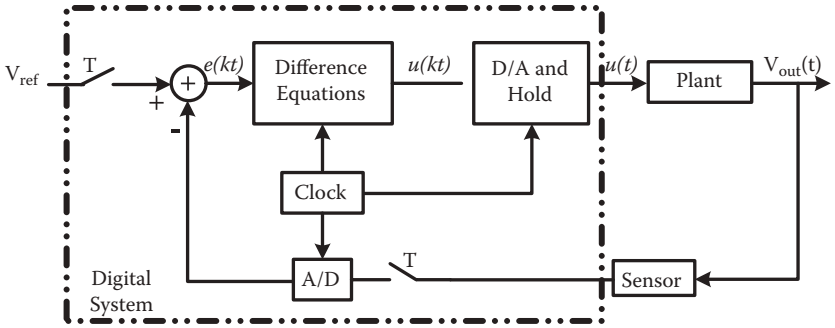


Figure 15.3 Average current mode control.

The inner loop subtracts a scaled version of the inductor current from the current program level. It then amplifies the resulting error and compares it to a sawtooth waveform to obtain the converter duty ratio. Any changes in the up and down slopes of the inductor current therefore directly influence the duty ratio. The outer loop subtracts the output voltage from a reference and amplifies the error to provide the current program level for the inner loop. Current and voltage controllers allow tuning of the inner and outer loops, to ensure converter stability and to achieve the desired transient response.

Digital current mode control employs a more basic method of realizing the inner current loop. It exploits the linear nature of the inductor current up and down slopes in the three main types of PWM converters.

A digital processor reads in samples of the maximum and minimum values of inductor current waveform for a particular converter. These are obtained by analog-to-digital conversion. The processor then calculates the average inductor current, over each switching cycle, via equation (15.14):

$$I_{ave}(n) = \frac{1}{2}[(I_{\min}(n) + I_{\max}(n))D(n) + (I_{\min}(n+1) + I_{\max}(n))D'(n)] \quad (15.14)$$

where, duty ratio $D(n) = t_{on}(n)/T$ and $D'(n) = 1 - D(n)$.

The processor then subtracts I_{ave} from the current program level and digital filters and scales the result to obtain the duty directly. It *also* reads in samples of output voltage each cycle. These are subtracted from the voltage loop reference and are digital filtered to obtain the current program level. In this way, the digital processor carries out the entire control strategy in software [18]. The authors of References 36 and 37 presented a new estimative current mode control technique for DC-DC converters operating in DCM.

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15.5.2 Predictive Control

The design of a feedback control law for switched-mode applications has been mainly based on linear control theory. In this approach, a linear approximation of the switched-mode circuit is first derived and then this linear approximation is used to design the control law. Thus, the design method is effective because of the fact that the switching frequency is often much higher than the bandwidth of the control loop. This high ratio of switching frequency to control bandwidth effectively decouples the control dynamics from the switching dynamics. For higher power applications, it is desirable to increase control bandwidth while maintaining a low switching frequency. As the ratio of switching frequency to control bandwidth decreases, the linear approximation of the switching circuit deteriorates and, consequently, the linear control law derived from such an approximation may not provide satisfactory performance. One solution to this problem is to include the switching dynamics in the control law. In each switching interval, the on-off state of the input switch(es) should be selected in such a way that the error between the next state (a predicted state) and the reference state is minimized [13].

Predictive control is based on the delta modulation method. In predictive control the input switch position is selected so that the state of the switched-mode circuit is driven closer to the desired state at the end of each sampling period. The selection of input switch position is then carried out. For each possible input switch combination, the predicted final circuit state is calculated based on the circuit model. The input switch position that produces a final state closest to the desired state is applied over the sampling interval. Figure 15.4 shows a block diagram of a switched-mode circuit, with k possible combinations of on-off states of the switch(es), operated by a predictive controller. The system consists of four functional blocks: the switched-mode circuit, a reference state generator, a state predictor, and a switch position selection. Functions of these blocks are described below [13].

1. *Switched-mode circuit*: The circuit includes power switching devices, reactive elements, and the load. The control input to this block is the position of the switch. In the case of a single-switch circuit, the input is simply either on or off. In inverter applications where more than one switch is used, the input can be one of several on-off combinations. Other possible external inputs (e(n)) to these circuits are, for example, back emf (in motor drive applications), grid voltage (in four-quadrant converter applications), and input DC voltage level (in DC-to-DC applications).
2. *Reference trajectory generator:* The reference trajectory generator generates a series of reference states (i.e., the reference trajectory, Xr)

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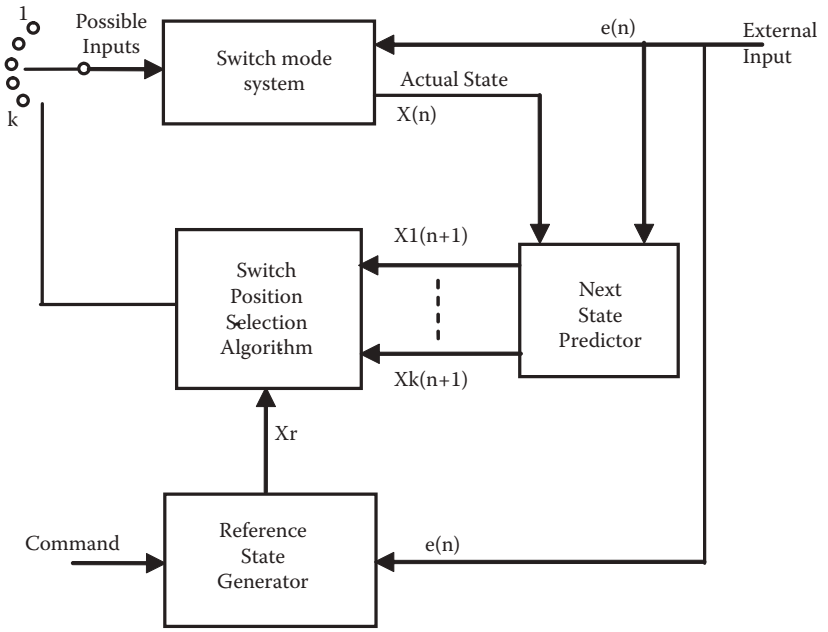


Figure 15.4 Predictive control system structure.

for the circuit to follow. The dimension of the reference trajectory should match the order of the circuit. In the case of a motor driver, for example, the reference trajectory includes the desired machine flux and the phase current. One way to generate a multidimensional reference trajectory from a scalar input command is to use a model of the switching circuit in conjunction with a feedback algorithm as shown in Figure 15.5. In this figure, the circuit model is a discrete time model of the switched-mode circuit. Note that unlike the input of the actual switched-mode circuit, the input to the circuit model is not limited to a number of discrete switch states. The model controller in Figure 15.6 is an algorithm that forces the control variable (yr) to follow the command. In doing so, a multidimensional reference state trajectory (Xr) is generated. In the case of the inverter application, the command is, for example, the desired output current. In DC-to-DC applications, the command input is the desired output DC voltage and the external input is the input voltage and load current.

Since the input to the circuit model is an analog value, the controller can be designed using any control theory. One should note that the model controller has no direct effect on the actual circuit The purpose of the model controller is merely to generate a feasible and well-behaved state trajectory.

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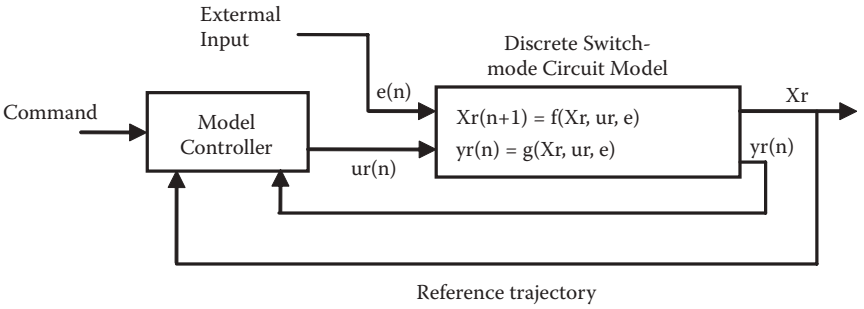


Figure 15.5 State feedback-based trajectory generator.

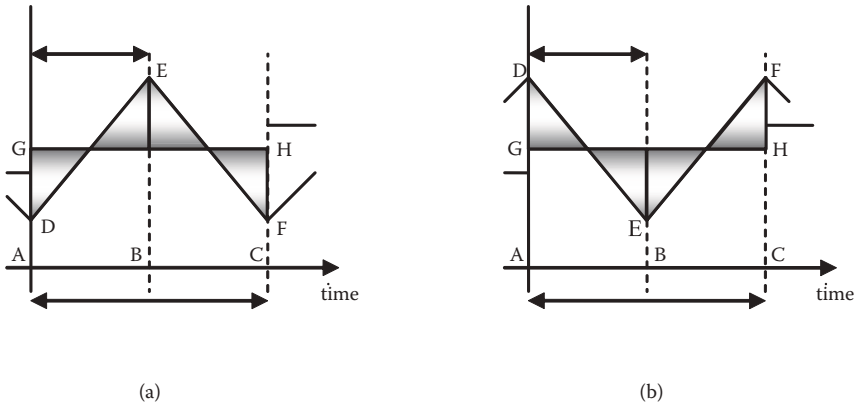


Figure 15.6 Reference and actual input current waveforms in method B. (a) Mode sequence I, (b) mode sequence II.

3. *Next state predictor:* The predictor calculates the state of the switched-mode circuit at the end of the sampling interval for each of the possible input switch combinations. In the case of a single-switch circuit, the predictor calculates two final states: the state with the switch open and the state with the switch closed. For a three-phase inverter, there are seven possible switch combinations; therefore, there are seven states to be calculated. The calculation of the next state is based on the discrete time model of the switched-mode circuit and this model may include nonlinear effects such as magnetic saturation or discontinuous conduction. The computer delay can also be considered and accounted for in the prediction algorithm.
4. *Switch position selection:* This algorithm compares the reference trajectory (Xr) against the states generated by the predictor. The input

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switch state that produces a circuit state vector closest to the reference state at end of one sampling period is the one that will be selected as the actual switch combination over the sampling period. The design parameter for this selection algorithm is the definition of closeness of two state vectors. In multidimensional cases, different weighting can be used for each state variable. The weights have an effect similar to state feedback constants.

In Reference 38, predictive control is used to control phased-controlled rectifiers. The authors of Reference 39 have selected predictive control for an equal charge criterion (ECC) scheme for a power factor correction (PFC) boost converter. In the proposed method, the on time $\left(t_1 - t_2\right)$ is determined such that ECC will be satisfied over the cycle period T_s, $\left(t_1 - t_3\right)$. Two ways of implementation (mode sequences I and II) of this control method are possible (Figure 15.6a and b). The following explanation is made with reference to mode sequence I (Figure 15.6a). A similar explanation can be made for mode sequence II by interchanging the roles of device sets (1, 4) and (2, 3).

In Figure 15.6a, device set (2, 3) is switched on at the start $\left(t_A\right)$ of the switching cycle of period T_s, followed by (1, 4) at time t_B. As stated earlier, the control method predicts the value of T_{ON} such that the ECC is satisfied at the end of the cycle. Thus,

$$\int_{t_A}^{t_C} \left(i_{act}(t) - i_{ref}(t)\right) dt = 0 \tag{15.15}$$

The assumption of constant input AC voltage during the switching cycle results in linear variations as shown.

With mode sequence I, in the positive line-current half cycle, the inductance L charges up first and then discharges into the DC bus. However, in the negative half cycle with the same sequence, the inductor first discharges as it drives current against the DC bus and then charges. In mode sequence II, the sequence of inductor charging and discharging during the positive and negative line-current half cycles is reversed. By setting the shaded area equal to zero, a quadratic equation in T_{ON} is obtained for each mode sequence.

$$aT_{ON}^2 + bT_{ON} + c = 0 \tag{15.16}$$

where

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$$a = -\frac{V_{dc}}{L}, \qquad b = -\frac{2V_{dc}}{L}T_s, \qquad and \qquad c = T_s(i_x - I_{ref}) + \frac{T_s^2}{2L}(V_{in} - V_{dc}) \tag{15.17}$$

for mode sequence I and

$$a = \frac{V_{dc}}{L}, \qquad b = -\frac{2V_{dc}}{L}T_s, \qquad and \qquad c = T_s(i_x - I_{ref}) + \frac{T_s^2}{2L}(V_{in} + V_{dc}) \tag{15.18}$$

for mode sequence II, where V_{in} and I_{ref} are the input AC voltage and reference input current for the switching interval, and is the current at the start of the interval (t_A). The control system must solve equation (15.16) in each switching cycle to obtain T_{ON}, which determines the switching instant within the period T_s.

In Reference 40, the predictive control approach was used in solving the quadratic equation for T_{ON}, keeping the appropriate device pair on for that duration in each switching interval. The authors of Reference 41 chose predictive control to control a PWM AC-DC converter, and in Reference 42 the predictive switching modulator (PSM) for current mode control of a high-power-factor boost rectifier is proposed.

The fact that in predictive control the inductor current is forced to follow the command current within one switch cycle creates several drawbacks of conventional current mode control, such as current loop instability and error between inductor peak current and command current. Advantages of predictive control mode (PCM) over the conventional current control mode (CCM) are as follows [40]:

- Its current loop is stable for any duty ratio D.
- It dispenses with the need of inductor current slope compensation, which is a must in CCM.
- Its control circuit can be easily implemented using wideband op-amps and an analog divider.
- It offers scope for active PF correction along with output voltage regulation at constant switching frequency.

15.5.3 Sliding Mode Control

The deadbeat control scheme has the disadvantages of being highly sensitive to parameter and load variations and requiring a large peak-to-average ratio of control signals to achieve the effect. The main advantage of the digital sliding mode control (DSMC) scheme is its insensitivity to parameter variations and load disturbances, which leads to invariant steady-state response in the ideal case, while its disadvantages are that it is not easy to

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find an appropriate sliding surface and its performance will be degraded with a limited sampling rate [9], [43], [44].

Many researchers have pointed their attention to the application of a sliding mode control (SMC) scheme to power converters through analog technique. Analog realization of the SMC has the disadvantages of complicated hardware design and limited control functions. Moreover, if the designed sliding mode controller is implemented by a microprocessor, the sampling action of finite frequency would violate the basic assumption of infinite switching frequency. The discrete sliding mode controller is robust to uncertainty and external disturbance. Thus, it can improve the transient response caused by the load variation. The results of DSMC are very different from those of the conventional analog sliding mode control theory. The most important difference is that the switching frequency of the control input of a discrete sliding mode controller is no longer infinite. The finite frequency operation makes the discrete sliding mode control algorithm available for a digital control system.

Discrete time-state-space dynamic equations of a PWM inverter can be expressed as

$$\begin{aligned} x(k+1) &= \Phi x(k) + \Gamma u(k) \\ y(k) &= C^T x(k) \end{aligned} \tag{15.19}$$

where u and y are scalar input and output of the system, respectively. To facilitate the analysis, we define another state vector as

$$e(k) = x(k) - x^*(k) = [v_c - v_{cd} \quad i_L - i_{Ld}]^T \tag{15.20}$$

where $x^*(k)$ is a vector that contains the reference signals of each state variable. The sliding surface is defined as

$$s(k) = G^T e(k) = g_1 e_1(k) + g_2 e_2(k) \tag{15.21}$$

Supposing that the reference signal keeps constant and bounded for all time, the so-called equivalent control can be derived as follows by letting $s(k+1) = s(k)$:

$$\begin{aligned} u_{eq} &= -\frac{1}{\alpha} G^T (\Phi - \mathrm{I}) x(k) \\ \alpha &= G^T \Gamma \end{aligned} \tag{15.22}$$

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G should be chosen such that the system controlled by u_{eq} is stable, that is, the closed-loop system must have all its eigenvalues inside the unit circle except the trivial eigenvalue $\lambda_m = 1$. Unlike the conventional analog sliding mode controller, the reaching and sliding condition for the discrete sliding mode control system is of the following form:

$$|s(k+1)| < |s(k)| \tag{15.23}$$

The discrete sliding mode control law can be designed as

$$u(k) = -\frac{1}{\alpha} G^T(\Phi - \mathbf{I})x(k) + \Psi^T e(k) - {}_0 s(k) \tag{15.24}$$

The feedback gain ψ and φ_0 is determined as follows:

$$\psi_i = \begin{array}{ll} F_0 & if \quad \alpha e_i(k)s(k) < -\delta_i \\ 0 & if \quad -\delta_i \,''\, \alpha e_i(k)s(k) \,''\, \delta_i \\ -F_0 & if \quad \alpha e_i(k)s(k) > \delta_i \end{array} \tag{15.25}$$

For *i = 1, 2*, where

$$\delta_i = \frac{F_0 \alpha^2}{2(1-\rho)} |e_i(k)| \bullet \prod_{j=1}^{n} |e_j(k)| \tag{15.26}$$

φ_0 must be chosen such that $0 < \rho < 1$. F_0 is a positive number and is constant for all time. In addition, F_0 is not arbitrary but is bounded by

$$0 < F_0 < \frac{2(1-\rho)|s(k)|}{|\alpha| \bullet \prod_{j=1}^{n} |e_j(k)|} \tag{15.27}$$

It follows from equation (15.27) that F_0 should be chosen as small as possible. A discrete feed-forward sliding mode control (DFSMC) scheme for the closed-loop control of a PWM inverter used in a UPS system is presented in Reference 42.

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15.5.4 Space Vector Control

Due to the complexity of power electronic equipments along with the availability of fast and inexpensive digital signal processors (DSPs), A/D and D/A converters, and other digital components, digital controllers are more commonly used in these applications. According to the nature of the input and output variables (voltages or currents), and depending on the direction of energy flow, three-phase converters can be dealt with as voltage source or current source inverters or rectifiers. The set of input or output variables in general consists of a three-phase current or voltage and a DC voltage or current, respectively. The function of high-frequency synthesis of the low-frequency converter waveforms can be defined as follows for a set of given input variables,

$$\begin{aligned} x_1 &= X_m \cos(\omega_x t + \quad_x) \\ x_2 &= X_m \cos(\omega_x t - 2\pi/3 + \quad_x) \\ x_3 &= X_m \cos(\omega_x t + 2\pi/3 + \quad_x) \\ x_4 &= X_{dc} \end{aligned} \tag{15.28}$$

and for a set of desired output variables,

$$\begin{aligned} y_1 &= Y_m \cos(\omega_y t + \quad_y) \\ y_2 &= Y_m \cos(\omega_y t - 2\pi/3 + \quad_y) \\ y_3 &= Y_m \cos(\omega_y t + 2\pi/3 + \quad_y) \\ y_4 &= Y_{dc} \end{aligned} \tag{15.29}$$

The purpose is to find the control law for the switches in Figure 15.7, so that the synthesized output variables have the same low-frequency part of the spectrum as the desired variables in equation (15.29).

For example, if the converter in Figure 15.7 is used as a voltage source rectifier (VSR), the input variables x_1 to x_3 are voltages v_1 to v_3, respectively, and x_1 is the current I_0. The output variables y_1 to y_3 are the phase currents i_1 through i_3, respectively, and y_4 is the voltage V_0. The phase current space vector modulated (SVM) converter in the VSR can be described as follows. Due to the voltage sources at the AC side and the current sources at the DC side of the rectifier, the converter switches may assume only six allowed combinations, which yield nonzero phase currents, and three combinations with zero phase currents. In the space

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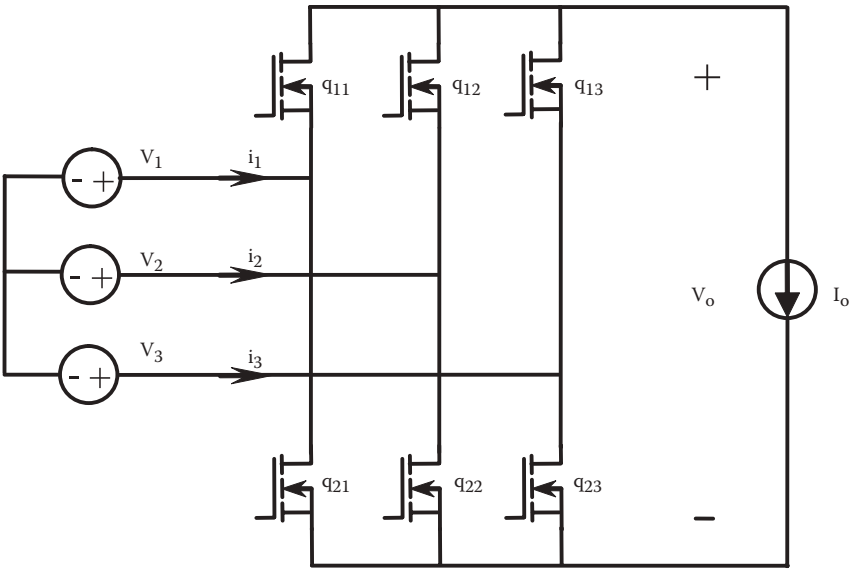


Figure 15.7 Voltage source rectifier.

vector representation, the input phase currents are therefore synthesized from seven discrete current vectors I_0 to I_6, also called the current switching state vectors (SSVs), as shown in Figure 15.8a. Numbers in parentheses indicate the switches q_{ij} in Figure 15.7, which are closed for the corresponding vector. The six SSVs form the VSR hexagon, and the triangular area between two adjacent SSVs is called a sector.

The space vector of the desired phase currents, $\underline{i}_{ref}$, called the reference current vector, can be approximated by its two adjacent SSVs and the zero vector using PWM. Since the operation within any sector is similar, the duty cycles of the three SSVs belonging to a sector that contains $\underline{i}_{ref}$ are

$$\begin{aligned} d_a &= d_m \sin(\neq / 3 - \theta_i) \\ d_b &= d_m \sin(\theta_i) \\ d_0 &= 1 - d_a - d_b \end{aligned} \tag{15.30}$$

where d_a, d_b, and θ_i are shown in Figure 15.8b, and $0 \text{ ″ } d_m \text{ ″ } 1$ is the modulation index. It can be easily shown that with these duty cycles, the local averages of phase currents are sinusoidal, and the voltage V_0 is DC, as desired [45].

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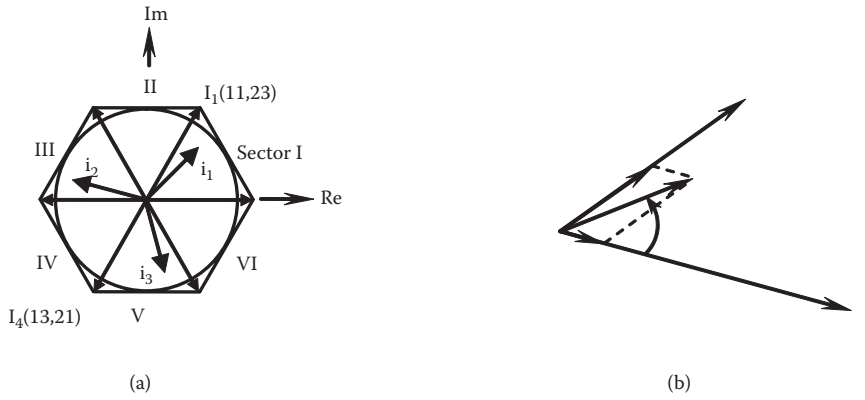


Figure 15.8 SVM in the VSR. (a) VSR hexagon, (b) VSR SVM vector addition.

The sectors of the VSR hexagon in Figure 15.8a corresponds directly to the 60° segments within the period of the desired phase currents. The angle θ_i in equation (15.30) is the angle from the beginning of a segment, and the duty cycles d_a and d_b can then be expressed as

$$d_a = d_m \frac{|i_a|}{I_{im}} \tag{15.31}$$

where i_a and i_b are the two desired input phase currents that have the same sign within the segment. Hence, each segment determines an operating mode of the VSR, i.e., the correspondence between {a, b} and {1, 2, 3}. It should be noted that the SSV duty cycles in equation (15.30) are not the duty cycles of individual converter switches, but of the switching combinations, which realize the corresponding SSVs. The duty cycles in equation (15.30) can be realized with several different switch-duty-cycle combinations, the choice of which is made on the basis of minimizing the converter switching losses. For this reason, it is often convenient to change switch-duty-cycle combinations that realize the SSVs at the middle of the 60° segments, when the variable $|i_a|$ in equation (15.31) becomes smaller than $|i_b|$. In this case, the operating mode of the converter is changed every 30°.

The SVM modulation scheme for inverter circuits is completely analogous to the SVM for VSR. The duty cycles in equation (15.30) are now determined by the desired output line voltages instead of desired input phase currents. So, instead of equation (15.31), the duty cycles are given by

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$$d_c = d_m \frac{|v_c|}{V_{om}} \tag{15.32}$$

where v_c and v_d are the two desired output line voltages that have the same sign within a given segment, and V_{om} is the desired output line voltage amplitude. This results in one significant difference in the controller implementation. In the rectifier circuits, the reference vector is always derived from the three-phase input quantity. For example, in the described VSR, it is desirable that the input phase currents are sinusoidal and in phase with the input phase voltages, i.e., the sinusoidal functions in equation (15.30) can be obtained from the input phase voltages. Alternatively, the sinusoidal functions in equation (15.30) can be generated internally by using look-up tables (LUTs), where the table readout must be synchronized with the input voltages. In the inverter, the frequency, phase, and magnitude of the synthesized three-phase quantity are somewhat arbitrary, so that the reference has to be generated internally, using an LUT.

From the above description of SVM, it can be summarized that a digital controller of an SVM converter has to perform the following tasks in every switching cycle:

1. Determine the operating mode of the converter according to the present segments of the three-phase input and output quantities
2. Calculate the duty cycles, *d,* for the switches to perform the required current and voltage synthesis tasks
3. Convert the duty cycle values into switching pulses of corresponding duration (PWM)
4. Distribute the pulses to the appropriate switches according to the present converter operating mode

The functional block diagram of a universal AC-to-AC SVM digital controller is shown in Figure 15.9a. The system controls both rectification and inversion simultaneously. The control process within each sampling interval starts by measuring the input phase voltages, v_1, v_2, and v_3, converting them into digital form, scaling them, and thus producing the scaled measurement of input voltages u_1, u_2, and u_3. Using this measurement, the present 30° segment of the input voltages is determined in the functional block SEG. The segment information is coded by a six-bit word (S_{i0} to S_{i5}), in which the lower three bits S_{i0}, S_{i1}, and S_{i2}, represent the signs of the line voltages v_{12}, v_{23} and v_{31}, and the upper three bits, S_{i3}, S_{i4}, and S_{i5}, represent the signs of the phase voltages, v_1, v_2, and v_3, respectively. The upper three bits of the segment information are used in the multiplexer (MUX) block to select the two input phase voltages with

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the same sign, u_a and u_b, which are, according to equation (15.31), used as current references, i.e.,

$$\frac{|i_a|}{I_{im}} \equiv u_a, \qquad \frac{|i_b|}{I_{im}} \equiv u_b \tag{15.33}$$

The segment information S_{o0} through S_{o5}, and the following references

$$\frac{|v_c|}{I_{im}} \equiv u_c, \qquad \frac{|v_d|}{I_{im}} \equiv u_d \tag{15.34}$$

for the calculation of the inverter SSV duty cycles in equation (15.32) are generated internally according to the input variable θ_o, which determines the desired frequency and phase of the synthesized output three-phase quantity.

The references u_a through u_d are combined and multiplied by the modulation index d_m, to obtain the switch duty cycles, d_a through d_d. This can be done in two different ways, depending on the converter topology, as shown in Figure 15.9b and c. If the cyclo-converter is implemented as a rectifier and the inverter is connected through a DC link, the duty cycles are generated as shown in Figure 15.9b. In this case, the rectifier and inverter controller functions are independent, each having its own modulation index input, d_{mi} and d_{mo}, respectively. If the cyclo-converter is implemented as a matrix converter, the rectifier and inverter references are combined and multiplied by a single modulation index, as shown in Figure 15.9c. The modulation index d_m (or d_{mi} and d_{mo}) and the output phase information θ_o are the inputs to the controller, and in general are supplied by the output regulation loops.

The calculated duty-cycle information d_a through d_d is sent to the PWM generators, which generate a coded switching instant sequence, *A* through *D*. The PWM signals *A* to *D*, and the operating mode signals S_{i0} to S_{i5}, are sent to the decoder, which distributes the gate-drive signals to the appropriate converter switches. The decoder also performs the converter shutdown in case of software failure, overcurrent, or overvoltage conditions, or external shutdown request.

The functions encircled by the dashed line in Figure 15.9a are performed by a DSP. The controller implementation and the division of controller tasks between software and hardware may vary, depending on the power stage topology and the components used in the controller implementation [45].

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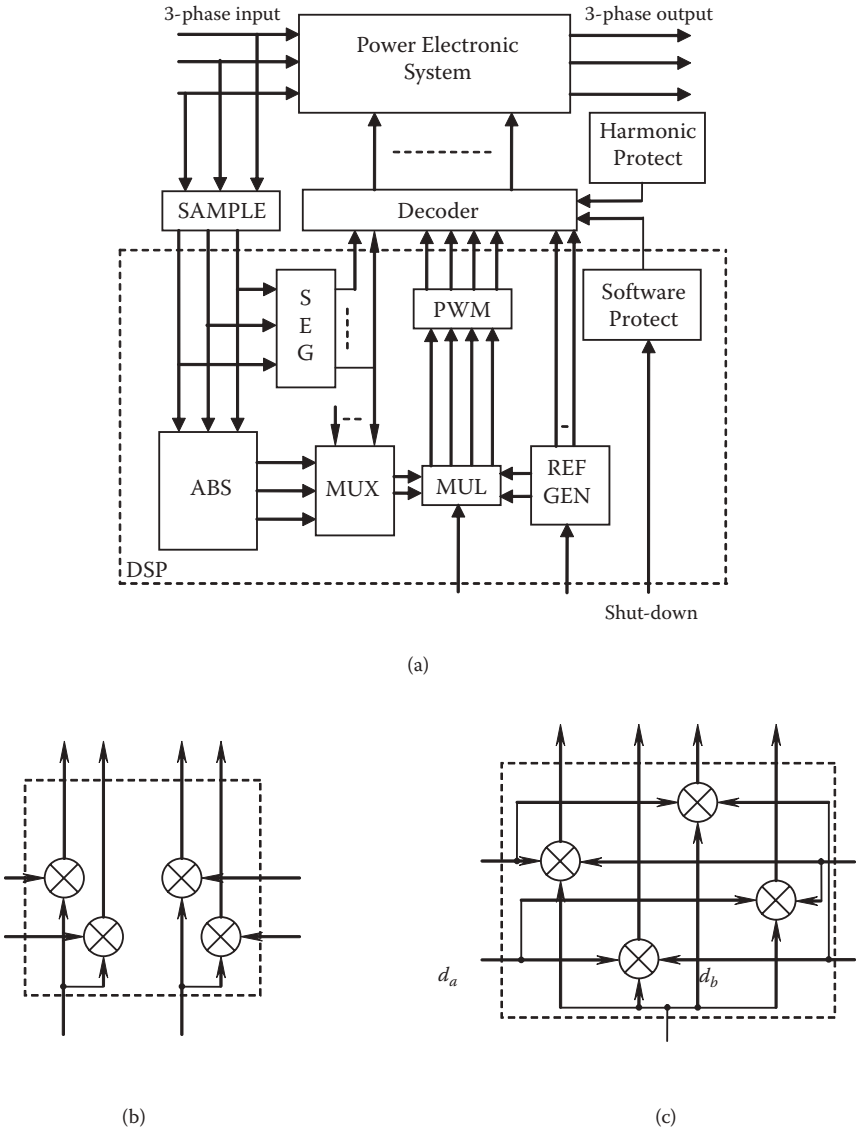


Figure 15.9 Controller functions. (a) SVM controller functional block diagram, (b) and (c) implementations of MUL block.

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15.5.5 Fuzzy Control

The fuzzy set theory introduced by Zadeh has found many applications in a variety of fields. Among the most successful applications of this theory is fuzzy logic control. A fuzzy logic controller consists of three major process blocks. They are (a) fuzzification, (b) rule evaluation, and (c) defuzzification. The block diagram of a closed-loop fuzzy logic control system is shown in Figure 15.10. The fuzzification process takes input values and combines them with stored membership function information to produce the grade of membership function. After the grade of membership function is produced, the fuzzy inference will evaluate rules. The truth value for each rule is the minimum of the fuzzy inputs for that rule, and this truth value is stored to each fuzzy output for that rule unless a larger value is already stored in the fuzzy output. When all fuzzy outputs are derived, the defuzzification is performed by combining all fuzzy outputs into a specific composite result to the system. With the availability of high performance DSP chips, most of the fuzzy processes can be done in only one instruction cycle [46]–[48].

15.5.6 Pulse Train Control Method

The pulse train digital technique to control DC-DC converters is introduced in references [49]–[52] and applied to flyback and BIFRED converters operating in discontinuous conduction mode (DCM). In contrast to the conventional analog control methods, the principal idea of this method is to use real-time analysis. The proposed technique is appropriate for any converter operating in DCM. The pulse train control algorithm regulates the output voltage based on the presence and absence of power pulses, rather than employing pulse width modulation (PWM). If the output voltage is higher than the desired level, *low-power sense pulses* are generated

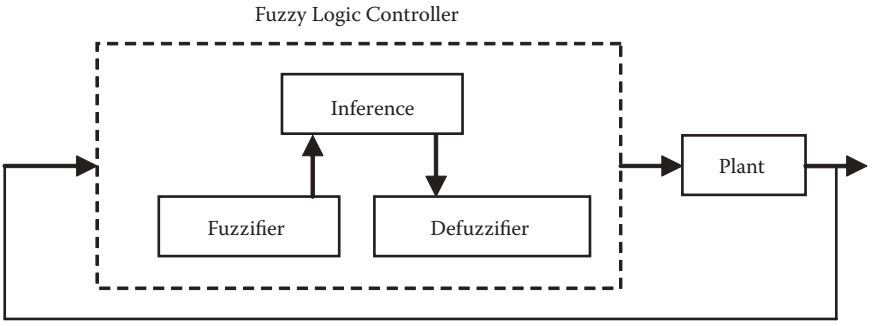


Figure 15.10 Block diagram of typical fuzzy logic controller.

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sequentially until the desired voltage level is reached. On the other hand, if the output voltage is lower than the desired level, instead of sense pulses, *high-power power pulses* are generated. At the beginning of each switching cycle, based on the difference of the output voltage with the desired voltage level, it will be determined whether a power or sense pulse needs to be generated. Operating in constant peak current mode control in a power pulse the switch remains on and the primary current is allowed to increase ,until it reaches a designated peak level $(I_{\max})$. At this point, the switch turns off and the next cycle starts when the secondary current reaches zero. A sense pulse has the same period as the preceding power pulse, but the switch turns off when its current reaches $I_{\max}/k$. Since the primary current ramps linearly with the switch on time, the switch on time of a sense pulse is $1/k$ times that of the switch on time of a power pulse. Therefore, a sense pulse only transfers $1/k^2$ times as much energy as a power pulse.

15.6 Applications of Digital Control

The increasing performance and reduced cost of digital circuits have made their application convenient for power electronic applications. Some of these applications are DC-DC converters, motor drives, PWM generation techniques, power factor correction applications, electronic ballasts, distributed power systems, and standby power supplies. In this section these applications are reviewed.

15.6.1 Pulse Width Modulation

Pulse width modulation (PWM) schemes for power conversion have received much attention recently. Many PWM schemes have been developed and implemented successfully for different applications. Many recent PWM schemes are microprocessor-based and can be optimized for the minimization of harmonics power electronic applications. Here, different PWM techniques that can be implemented using digital systems are reviewed.

15.6.1.1 Naturally Sampled PWM

Naturally sampled PWM is the most standard and widely used PWM technique. In this approach a sinusoidal modulating signal is compared with a triangular carrier signal to produce the PWM signal. The instantaneous real-time intersection of these two signals determines the PWM switching instant by a process of natural-sampled PWM. Natural sampling PWM is nonlinear and the PWM pulse widths are defined by transcendental equations, which can only be solved using Bessel function series or numerical

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methods. Implementation of this method in digital applications creates some difficulties.

15.6.1.2 Regularly Sampled PWM

The above-mentioned difficulties associated with the natural PWM technique can be solved using the regularly sampled PWM technique. In this approach, a simple trigonometric equation is used to calculate the PWM pulse widths in real time using a software algorithm. The detailed description of this method is presented in Reference 53. This approach regularly spaces the PWM pulse positions and the pulse-widths are precisely defined such that it is impossible to drive a simple trigonometric equation to calculate the PWM pulse widths, which for a sinusoidal modulating wave is as follows:

$$\tau_K = \frac{T}{2}\ 1 + \frac{M}{2}(\sin(\omega t_K) + \sin(\omega t_{K+1})) \tag{15.35}$$

where

$$\tau_{K+1} = t_{K+1}\frac{T}{2}, t_K$$

and t_{k+1} represent the sampling time instants, T is the carrier period, and M is the modulation index. This equation can be used directly to generate regularly sampled PWM in real time using a software algorithm. The regular-sampled PWM microprocessor approach has eliminated the need for any off-line calculations or extensive use of LUTs and interpolation between LUTs for voltage control providing wider industrial application.

Optimal techniques are also introduced in the literature [53], [54]. The author of Reference 53 proposed a technique that uses non-sinusoidal modulating wave samples. With suitable selection of the modulation wave, this technique can be simply extended to allow harmonic minimization and also harmonic elimination PWM to be closely reproduced using simple algebraic equations, which can be solved on line with a DSP. It is recognized that harmonic elimination and harmonic minimization of PWM strategies can offer significant advantages, particularly at low switching frequencies where the load harmonic losses can be considerably reduced with minimum inverter switching losses. Using this optimal microprocessor-based PWM technique, it is possible to produce optimized PWM inverter drive, uninterruptible power

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supply, and static frequency converter performance up to quasi-square wave operation.

These techniques can be implemented on a carrier-cycle basis using both four-timer and single-timer microprocessors with the minimum of on-line calculations. An alternative approach uses the special characteristics of three-phase waveforms to simplify the microprocessor implementation [55].

15.6.1.3 Randomly Sampled PWM

As mentioned earlier, the PWM signal is produced conventionally by comparing a sinusoidal modulating signal with a triangular carrier signal. In general, traditional PWM schemes provide a PWM waveform with a large fundamental voltage component with low-order harmonics suppressed. However, the harmonic power is usually concentrated in the high-frequency range due to the high-frequency switching of the power inverter. These high-frequency harmonics can have adverse effects, such as acoustic noise, harmonic heating in electric machines, and radio interference.

In Reference 56, random sampled PWM (RPWM) schemes based on the use of random number generation have been proposed for comparison with the fundamental sinusoidal waveform in order to generate RPWM waveforms. The randomness added into the PWM waveform can cause the harmonic power to spread over the harmonic spectrum so that no harmonic component has a significant magnitude. The resulting RPWM spectrum effectively consists of large fundamental components with both low- and high-order harmonics suppressed. The RPWM approach offers advantageous features such as reduced radio interference from converter equipment and improved acoustic and vibration effects in electronic drive systems. In each RPWM scheme, the random number generated is compared with a sinusoidal reference signal at a certain sampling frequency. The result of this comparison forms the digital RPWM signal. Most of the early RPWM schemes employ a very high frequency (ranging from 60–480 kHz) for the random number generation, resulting in corresponding high inverter switching frequency (15–25 kHz), which is only suitable for MOSFET-based inverters and not for insulated-gate bipolar transistor (IGBT) inverters. Several RPWM schemes have been developed. We present a few major methods for random number production [44].

15.6.1.3.1 Mathematical RPWM. (MRPWM) is based on a mathematical equation that can generate a random number. The general form of the random number equation is as follows:

$$R_{n+1} = \mathrm{mod}_{Ns} |R_n{}^* P_1 + P_2| \tag{15.36}$$

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where R_{n+1} and R_n are the random numbers at the $(n+1)^{th}$ and n^{th} step, respectively. P_1 and P_2 are prime numbers, and *Ns* is the number of bits for number representation. This approach is very suitable for microprocessor implementation because it involves only one multiplication and one addition along with the modulus operation. Various pairs of prime numbers P_1 and P_2 can be employed.

15.6.1.3.2 Logical RPWM is based on the logical operation of several bits of a digital binary number and is commonly known as a pseudo-PWM code generator in communications. By first performing certain logical operations on several bits, the modular-2 operation of these bits forms a new bit value. By shifting the binary number by one bit with the new bit forming the least significant bit, a new binary number is then generated. The number generation is known as pseudo-random number generation because the random number pattern is repetitive. This approach simply requires XOR and shift operations, and is therefore suitable for real-time microprocessor implementation. The logical RPWM (LRPWM) generation, in principle, can be developed by different numbers of bits. Figure 15.11 shows a 14-bit implementation.

15.6.2 Motor Drives

Recently digital control has found many applications in motor drive systems. In Reference 57, digital control is used in a motor drive application to control a high-speed elevator. In this application three microprocessors were used to generate the required PWM signals as well as a detection and protection system for abnormal over-voltage conditions. This system is comprised of a converter to convert the constant frequency AC power from the power source to DC power, a DC reactor (Ld) to smooth the DC

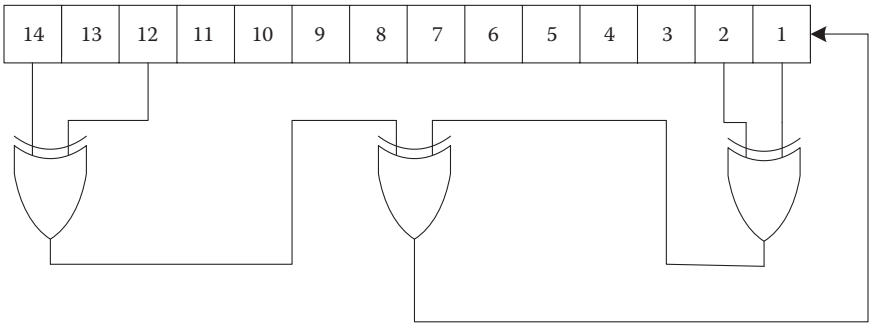


Figure 15.11 Logical arrangements for pseudo–random number generation for 14-bit system.

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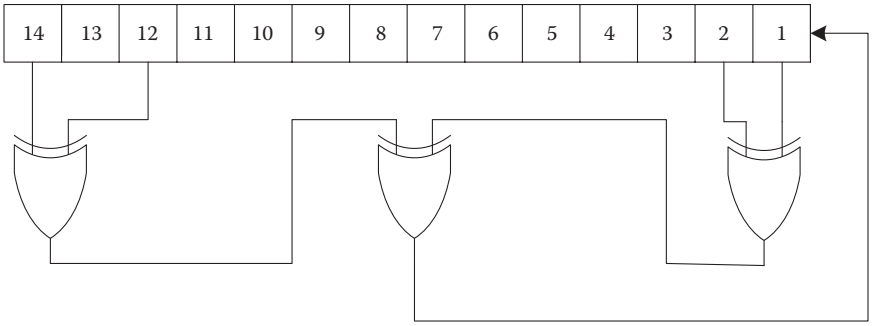


Figure 15.12 Control circuit block diagram.

current, and an inverter to convert the DC power to the variable-voltage variable-frequency AC power, as shown in Figure 15.12.

In this application two exclusive on-chip microprocessors (for the inverter and converter units) generate the PWM control signal without an external logic circuit. In other words, both converter and inverter units require PWM control to produce the sinusoidal voltage and current. In addition, the converter part uses DC-link voltage control to regulate the magnitude of the induction motor current, whereas the inverter part utilizes the frequency and phase control corresponding to the motor speed. Figure 15.12 is a block diagram of the control circuit. The automatic speed regulator (ASR) and management of the various elevator signals are executed by the main 16-b microprocessor (CPU-0). The main microprocessor generates a DC current instruction, a frequency instruction, and a phase instruction by employing ordinary vector calculations. The automatic DC current regulator (ACR) is executed by the exclusive 16-b one-chip microprocessor (CPU-1) with PWM control. Input signals for CPU-1 are the deviation signal between the current instruction and DC current and the synchronization signal.

15.6.3 Power Factor Correction

The typical power factor correction (PFC) converter has three control loops: the inner current loop, the line voltage feed-forward loop, and outer voltage loop [46]. The average output DC voltage is regulated by a slow response outer loop, whereas the inner loop that shapes the input current is a much faster loop. However, due to the poor open loop line regulation when operated in a wide input range and the limitation of control loop bandwidth, typically, an input voltage feed-forward loop is included in the control system and it is the slowest loop. The outer voltage loop regulates output voltage for a given reference. Since the

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output voltage contains a large second harmonic (120 Hz) ripple, the low bandwidth controller has to be designed to ensure the input current command is not affected by this second harmonic ripple. The crossover frequency of a typical controller design is at most 20 Hz, which produces a poor step load response. Any increase in the crossover frequency would increase the input current distortion to an unacceptable level. In order to increase crossover frequency without increasing input current distortion, a sample and hold circuit (S/H) can be used. By putting an S/H circuit in the outer voltage loop, the output voltage control loop becomes a sampled data system and a high dynamic performance outer voltage loop with a digital controller can be designed. The control system including feed-forward path and an S/H circuit is shown in Figure 15.13.

In Reference 46, a fuzzy logic control (FLC) and a digital proportional and integral (PI) control are proposed for the application in feedback control of a PFC pre-regulator used in a high performance on-line uninterruptible power supply (UPS). Since the performance of a fuzzy logic controller only depends on the selection of membership functions and the inference of fuzzy rules, and fuzzy set theory, in nature, is capable of working with nonlinear systems, fuzzy logic controllers have an advantage in coping with the time varying nonlinearity of switches in the PFC pre-regulator, and do not require an accurate mathematical model of the PFC pre-regulator when the controller is designed. On the other hand, the digital PI controller algorithm is simpler and execution time is faster and it takes less software code space, but it needs an accurate mathematical model of the plant and it failed to perform satisfactorily under parameter variation, nonlinearity, load disturbance, etc. The simulation results of Reference 46 show that the fuzzy logic inference-based controller can

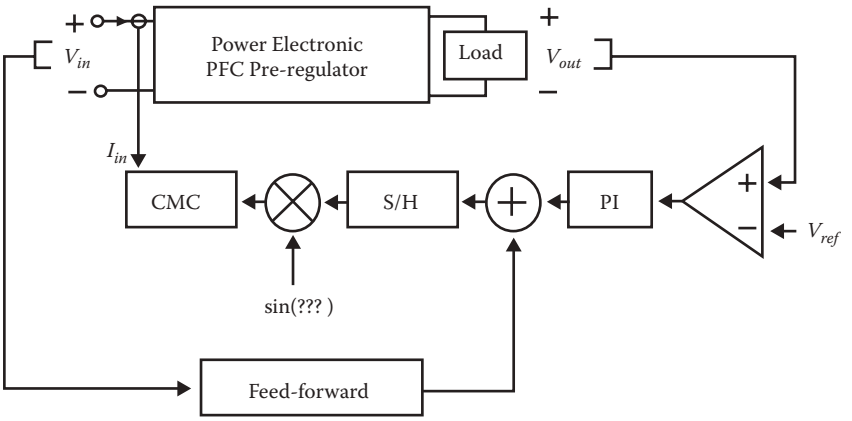


Figure 15.13 PFC control with feed-forward and S/H.

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achieve better dynamic response than its digital PI counterpart under large load disturbance and plant uncertainties.

15.6.4 Standby Power Supply with Active Power Filter Ability

The real-time digital control techniques using microprocessors or digital signal processors (DSPs) are becoming more popular in power electronic applications. Recently, utility power quality has become an important issue for critical loads such as computers and delicate electronic instruments. The UPS system can supply high quality power to keep the power sources of these devices from disturbances of noise and power outage. The authors of Reference 58 present a standby power supply/active power filter (SPS/APF) system. This system provides combined functions of high efficiency power backup and harmful harmonics elimination. Based on the bilateral converter using a current-forced switching scheme, the line current can be sinusoidally regulated with unity power factor in APF mode and the voltage waveform distortion can be kept small in SPS mode by instantaneous voltage control.

A bilateral converter system is shown in Figure 15.14. The rectifier mode controller and the inverter mode controller are automatically selected by the selector switch. In the rectifier mode option, the line current can be controlled sinusoidally with the unity power factor using the instantaneous current control techniques, and the DC voltage is regulated with low ripple. In addition, the sinusoidal AC output voltage with low harmonic distortion and good regulation characteristics in the inverter mode can be obtained using the instantaneous voltage control techniques.

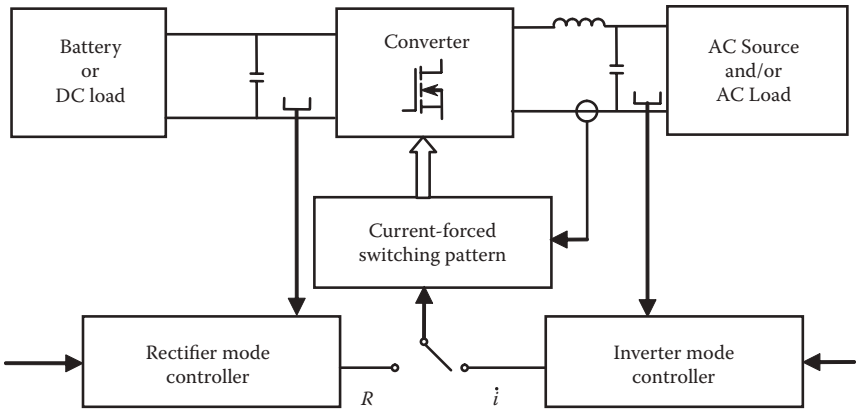


Figure 15.14 Control diagram of bilateral converter system.

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15.6.5 Distributed Power Systems

The block diagram of a typical distributed battery-backup power system employing several PFC converters connected in parallel is shown in Figure 15.15. This can be the power supply system for desktop PCs or servers. The architecture of Figure 15.15 has been used [59] for digital control of a single-phase, single-switch flyback PFC AC/DC converter. Active current shaping technique using the flyback converter was employed for the line harmonics control and DC voltage regulation of the 48-V power supply. The output voltage of this 48-V power supply can be backup, and voltage compensated by a battery-connected DC-DC converter under DSP-based digital control.

A DSP-controlled single-phase flyback PFC converter is adopted to realize such a distributed power supply system. The flyback PFC converter possesses characteristics of high efficiency (due to its single-stage, single-switch topologies), low cost, and galvanic isolation. The drawback of the flyback PFC converter is that it is only suitable for power level below 500 W. This drawback can be solved if we can parallel these converters using sophisticated control techniques. In order to let these AC/DC power modules be easily connected in parallel, an automatic current-sharing technique must be developed. This requires a wide bandwidth converter with a pseudo or a small output inductor. Traditionally, in order to maintain a sinusoidal input current, the closed-loop bandwidth of a PFC converter is required to be far below its rectified line frequency, which is double the line frequency for single-phase systems.

Figure 15.16 shows the proposed digital controller for the single-phase flyback PFC converter. A single-chip DSP controller was used for the realization of the proposed control algorithms. The proposed control scheme consists of four major parts: a current-loop controller, a nonlinear current reference, a voltage-loop controller, and a voltage ripple estimator.

15.6.6 DC-DC Converters

Another application of digital control is in DC-DC converters. Digital control has been applied to a DC-DC buck converter using an 8-bit microprocessor in [7]. In this application the applied controller is a digitally implemented PID type. A digital proportional-derivative (PD) controller is designed for a DC-DC buck converter [60]. Dynamic characteristics of digitally controlled DC-DC converters employing a PID controller are presented [61], [62]. The authors of Reference 63 designed an adaptive digital controller for switching DC-DC Ćuk converters. Results show that the computation speed of this method is slow and limited. Digital control of a boost PFC converter employing a digital PI controller was achieved [64], [65]. Analysis, design, simulation, and DSP-based implementation of

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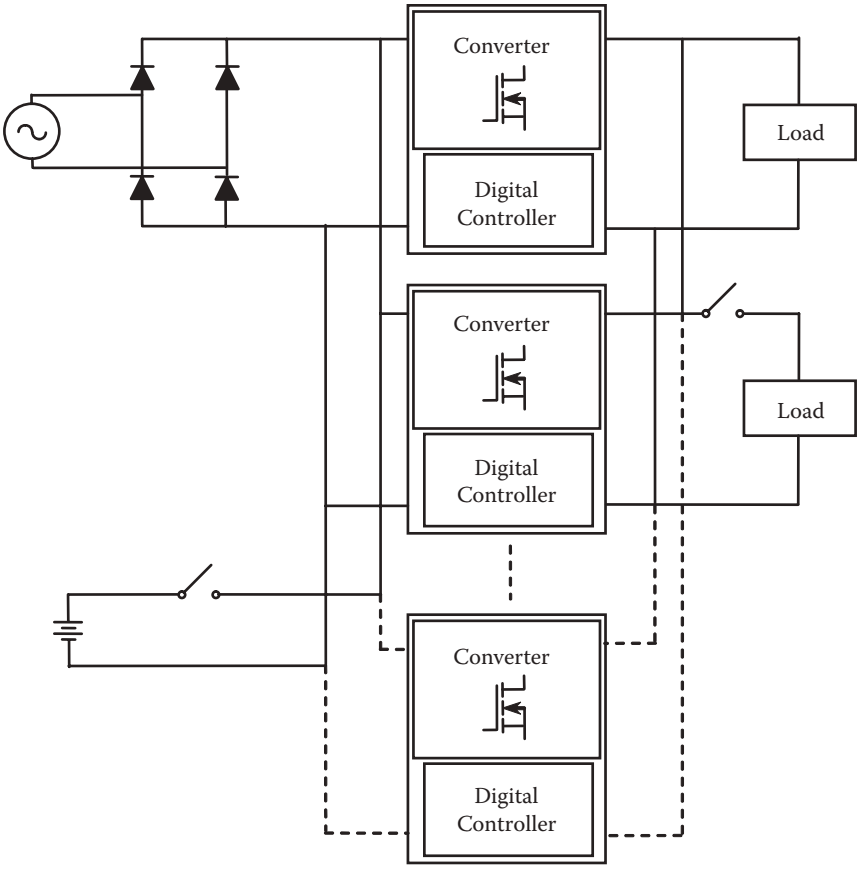


Figure 15.15 Distributed battery-backup power supply using digital control techniques for power factor control and automatic load sharing.

a digital controller using a Posicast element are presented in Reference 54 for the boost converter. Classical Posicast is a feed-forward control method used to cancel the oscillatory behavior of a lightly damped system. The block diagram of a boost converter employing Posicast is shown in Figure 15.17. In this figure *1+P(s)* is the Posicast element.

PID-based control of the power converter requires some algorithm modifications to achieve good transient and steady-state performance [60]–[66]. Digitally controlling the converter employing Posicast does not require any such modification. The frequency response of the Posicast element inherently reduced high frequency noise and avoided unfavorable effects on system stability caused by the RHP zero and parasitic elements in the dynamics of the converter.

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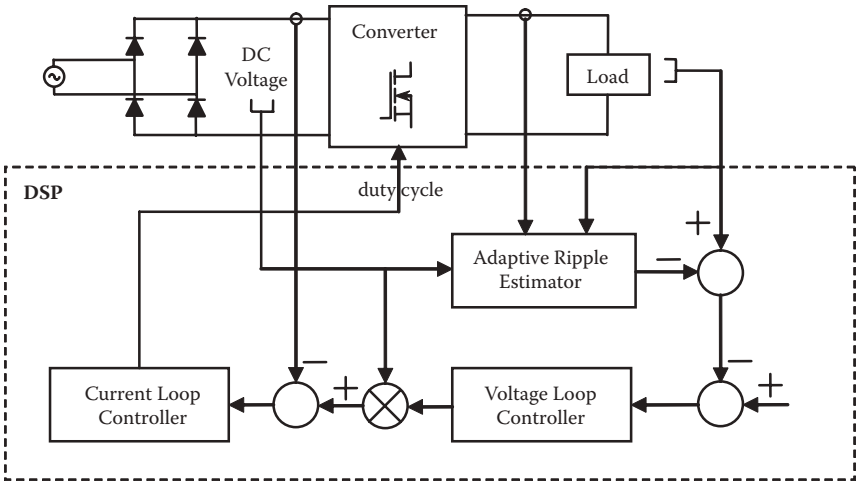


Figure 15.16 DSP controller for single-phase flyback PFC converter.

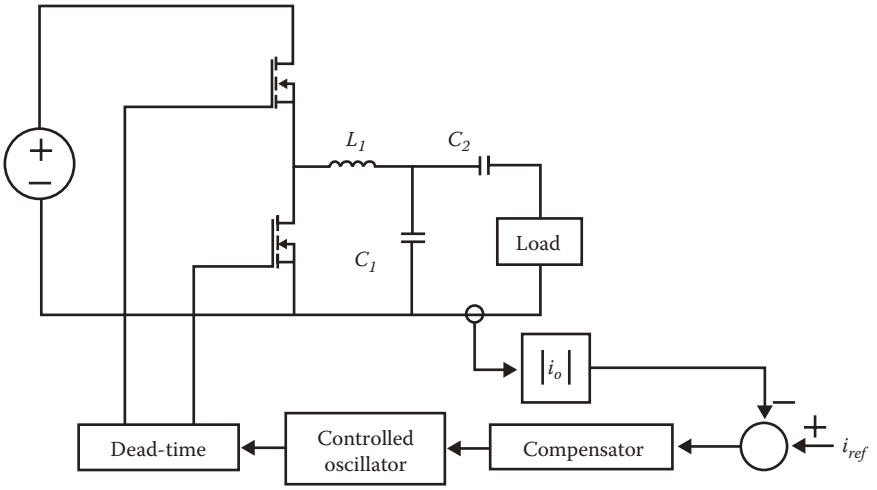


Figure 15.17 Block diagram of controlling power converter using Posicast.

15.6.7 Electronic Ballasts

Electronic ballast-based high-frequency resonant switching inverters, such as the example shown in Figure 15.18, are used to drive energy-efficient fluorescent lamps. Optimum ignition and dimming functions can be accomplished through active control, by varying the switching frequency. Robustness and simplicity of the controller are essential in ballast applications.

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For electronic ballast applications, direct digital phase control offers the advantages of self-tuning relative to the tank resonant frequency (insensitive to component variations), reduced sensitivity for improved control near resonance, and inherent protection against operation below resonance to avoid nonzero voltage switching conditions [53].

15.7 Implementation of Digital Controllers

There are different factors in the realization of a practical digital controller for power electronic systems. Major practical issues complicating the realization of a high performance digital controller include selection of the control processor, determination of the sampling rate, interfacing between the controller and the power circuit, hardware design, firmware design, and software realization of the control algorithms. These are not trivial tasks, and they need very careful design and practical perspectives. Software implementation plays a key role in designing a practical controller. It must be analyzed from a theoretical point of view with practical constraints. This is the key to a successful implementation of a digital controller.

Recently, two major approaches have generated the most interest in software implementation of digital control techniques. These are digital signal processor (DSP)-based and field programmable gate array (FPGA)-based programming techniques [67]–[70].

Digital control of a DC-DC boost converter operating in continuous conduction mode (CCM) was studied [68]. The digital control was

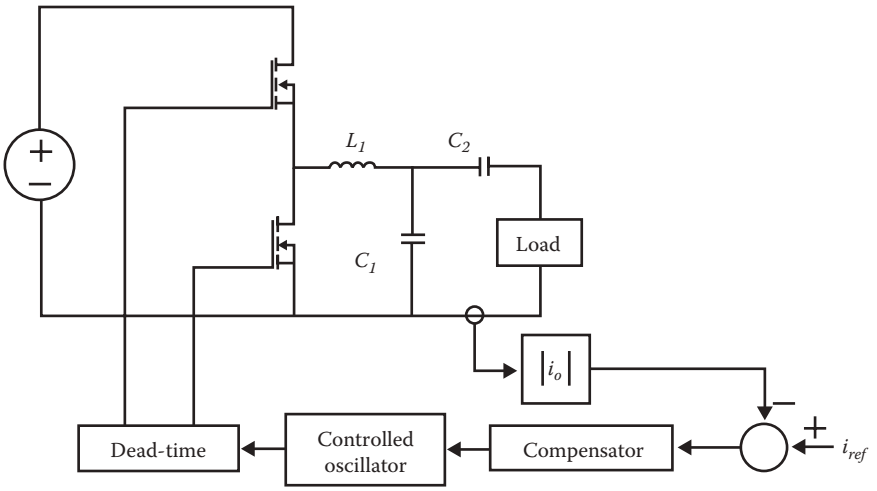


Figure 15.18 Electronic ballast.

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implemented in an FPGA using a hardware description language (VHSIC hardware description language [VHDL]). The authors of References 69 and 70 did a comparative analysis between DSP and FPGA-based control capabilities in PWM power converters. Moreover, the deadbeat control concept is implemented in a DSP as well as FPGA [69].

Mostly digital control of power electronic systems has been implemented in DSPs [71]. DSP-based controllers implement complex algorithms with many arithmetic operations. However, DSPs are not very common in high-switching-frequency or low-cost applications. PFC is no exception to this tendency and a few digital controllers have arisen for this application. Moreover, they are based on DSPs, exploiting their arithmetic resources.

The main limitation of DSPs is their sequential operation, that is, instructions are executed one after the other. However, DSPs have been adapted for power electronics applications adding peripherals such as PWM modules, general-purpose timers, and event interruption modules. These peripherals allow some concurrent operation, that is, several control tasks are performed simultaneously. The simultaneous tasks must be very simple (PWM operation, timing) and they are not sufficient for a general concurrent operation structures.

Following this tendency to use concurrent hardware for control purposes, a custom hardware solution is implementation of the digital control in an FPGA instead of a DSP in order to exploit its concurrent operation. All the internal logic elements of the FPGA, and therefore all the control procedures, are executed continuously and simultaneously. This method allows using high-speed demanding algorithms, like the digital charge control proposed [67] for the current loop. This method would not be possible using a DSP.

The control algorithms for FPGAs are usually developed using a hardware description language (VHDL). This method is as flexible as any software solution, like developing the control algorithms in C-language for a DSP. Another important advantage of VHDL is that it is technology independent [67], [68]. The same algorithm can be synthesized into any FPGA and even has a possible direct path to a custom chip. In this way, the FPGA could be substituted with an application-specific integrated circuit (ASIC), opening interesting possibilities in power systems in terms of performance and cost. VHDL has also been used for modeling purposes. The power converter and the A/D converters (ADC) have been modeled in VHDL in order to simulate the whole system. These models were designed simply in order to run long simulations in a reasonable time. In this way, both control loops, which differ greatly in their characteristic time, can be simulated simultaneously.

An FPGA-based solution changes the design point of view. Arithmetic operations should be kept to the minimum to optimize the required logic resources (silicon area). However, conditional execution (translated to *if*

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statements in VHDL) should be exploited because of FPGA's hardware-oriented nature.

Furthermore, it is shown [69], [70] that PWM ripple and high frequency rejection of the controller implemented in the FPGA in comparison with the controller implemented in the DSP are very high, ensuring robust regulation immunity to the non-idealities. Moreover, because of the parallel processing capability of FPGA, the computation time is faster than that of DSPs.

A disadvantage of FPGAs is their cost. They are slightly more expensive than DSPs and they have no A/D converters integrated, so their cost must be added. However, the high-speed A/D converter used in the proposed control can not be substituted by those usually integrated in the DSPs. The cost disadvantage would disappear by substituting the FPGA with an ASIC suitable for mass production.

15.8 Summary

A comprehensive study of digital control of power converters was presented. Advantages and disadvantages of digital control, digital control techniques, and their application implementations were discussed. Furthermore, different digital approaches were presented. DSP-based and FPGA-based implementation of digital systems were compared, and based on the literature, it was concluded that substituting the common DSP solutions with FPGA-based ones means a trade-off between the DSP capacity for arithmetic operations and the FPGA concurrency. In order to exploit the FPGA concurrency new control algorithms must be developed, because adapting the DSP ones to FPGAs would create no special advantage. These new algorithms can be quite simple, like the digital charge control proposed, but they must be designed from the concurrency point of view.

As for future work, a new digital control technique, which will be introduced in the next chapter, will be applied to control of DC-DC converters loaded by constant power loads (CPLs), and the simulation outputs as well as analytical results will be experimentally verified. The method will be comprehensively studied with the existing analog and digital control schemes. Cost, ease of implementation, simplicity, and functionality of the new method will be the concepts on which the future work will be focused.

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chapter sixteen

Implementation of Digital Control Using Digital Signal Processors

The control based on programmable digital devices such as programmable logic devices (PLDs), microprocessors/controllers (henceforth, μ-controllers), and digital signal processors (DSPs) is used widely for numerous applications ranging from home appliances to industry products. DSPs are adopted for system controllers due to their fast operation speed through dedicated arithmetic units with multipliers and fast analog-to-digital converters and digital-to-analog converters. Their fast operation is thought to be suitable enough for replacing the existing analog controllers. Of course, there are still intrinsic limitations in a digital controller's bandwidth, compared to the classical analog controllers. In many applications, however, system designers can select either appropriate μ-controllers or DSPs with enough performance. In addition, programmable controllers provide the flexibility of easily implementing unexpected conditions.

In general, in order to properly utilize DSPs as well as μ-controllers, designers should take a series of steps toward gathering the physical information about the chosen processor, software development environment, and interface between the processor and external circuits. The next step is to move on to actual implementation of the system. This chapter is intended to explain and provide helpful guidelines for implementation of a system controller based on programmable digital processors specifically with DSPs. For the convenience of explaining and understanding, a controller for a non-inverting buck-boost DC/DC converter [1]–[16] is presented. Some parts of the source codes and physical waveforms are provided.

16.1 Introduction to Implementation of Digital Control Based on DSPs

As the first stride toward the implementation of controllers using DSPs, the basic concepts of DSP in a hardware and software point of view, specification of the desired system, description of control flow based on the functional requirements, selection of proper μ-controllers or DSPs, and detail datasheets and manuals are explained.

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16.1.1 Basic Concepts of DSPs from Hardware and Software Points of View

DSP has two meanings based on hardware and software points of view. In terms of hardware, literally, a digital signal processor is a kind of μ-processor.

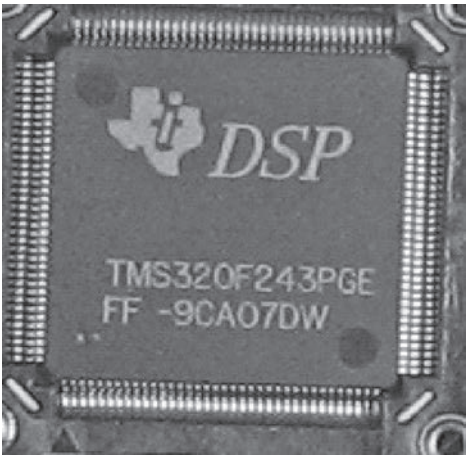
DSPs manufactured by various semiconductor companies are presented in Table 16.1. The examples of DSP chips supplied by manufacturers are shown in Figure 16.1. The chips have leads to exchange digital or analog signals with external circuits. The chips are soldered on printed circuit boards (PCBs). Once DSP chips are powered, they begin to execute

Table 16.1 DSP Hardware Manufacturers

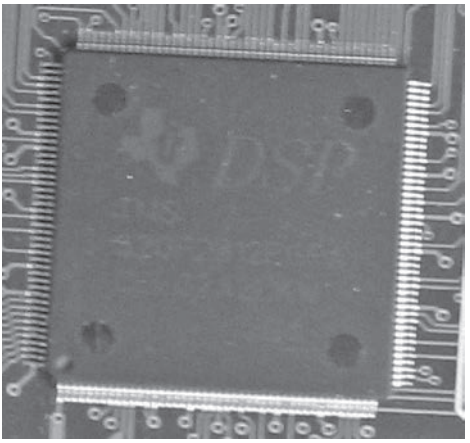
Manufacturer	Remarks
Advanced Devices, Inc.	16/32 bit/floating point
Advanced RISC Machines	(ARM) CPU core vendor
Analog Devices	16/32 bit DSP–SHARC
AverLogic Technologies, Inc.	
DSP Group	
Freescale Semiconductor, Inc.	32-bit embedded processors–uP/68000–uCRISC/DSP combo ICs
Hyperstone	RISC/DSP combo ICs
IDT	Packet classification processors
Infineon Technologies	
Intersil	8/16 bit CMOS uP
Intrinsity, Inc.	
Logic Devices	DSP devices
LSI	
MicroChip	dsPIC 16-bit RISC digital signal controllers
NXP	
STMicroelectronics	
Texas Instruments, Inc.	TI320Cxx DSP processors-high speed CMOS signal processing/all-digital down/up-converters, digital filters, high-speed QAM modem chip sets
VeriSilicon	DSP coprocessor, VoIP
Vitesse Semiconductor Corporation	DSP-based T3/E3 transceiver
Zilog	16-bit multi-purpose DSP manufacturer

Source: Davis, L. 2008. DSP processor vendors. http://www.interfacebus.com/Digital_Signal_Processor_Manufacturers.html.

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(a) TMS320F243PGE



(b) TMS320F2812PGFA

Figure 16.1 DSP chip (manufactured by Texas Instruments) examples.

the codes programmed by the designers in phase with the clock signals from crystal oscillators or resonators.

From a software perspective, digital signal processing is said to be DSP, which means a series of procedures composed of algorithms and software codes. In other words, DSP is about how to obtain the system desired analog/digital output signals from the analog/digital input signals. The procedures of DSP can be summarized as

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1. Capturing analog/digital input signals (sample and hold) from hardware pins through external interface circuits
2. Acquiring the digital data from the sampled signal through an analog-to-digital converter (ADC)
3. Carrying out operations and calculations with the converted data and making digital results—either integer, fixed point, or floating point calculations
4. Converting the digital results into the system desired analog signals through digital-to-analog converters (DACs) or digital output ports

Figure 16.2 presents overall flows of program execution procedures after the DSP chip is powered. Figure 16.3 shows a diagram explaining digital signal processing including the DSP chip and the mounted DSP user program.

16.1.2 *Specifications of Desired System*

The non-inverting buck-boost DC/DC converter is used as an implementation example. The first step is to specify the functional requirements. Clarifying the specifications is the most important job for designers.

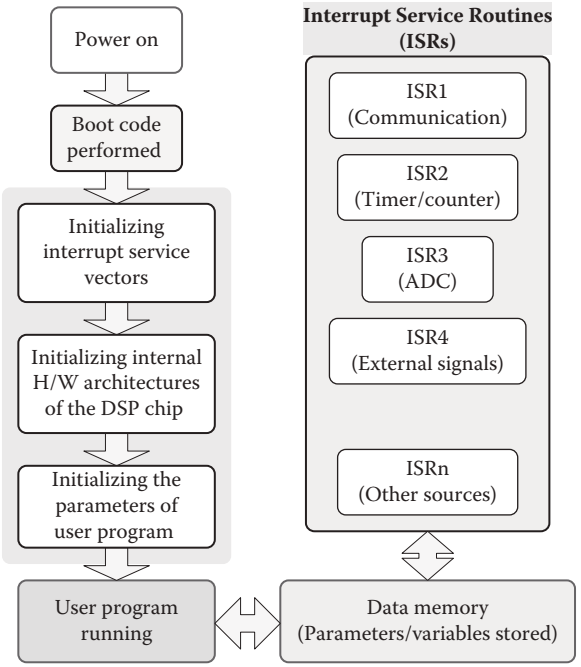


Figure 16.2 General flow of source codes execution on DSP chips.

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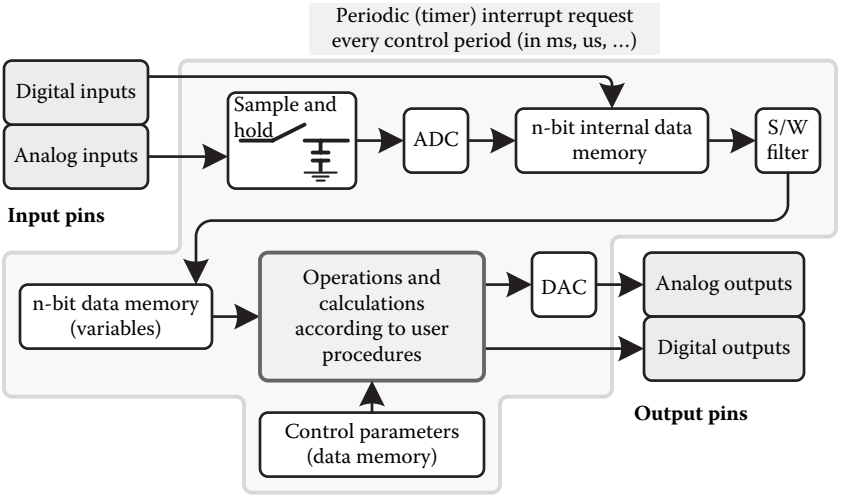


Figure 16.3 Overall flow of digital signal processing.

Through specifications, designers can break the project into sub-projects and assign individual jobs to team members. This helps integrate and evaluate the individual jobs.

16.1.2.1 Functional Requirements of Non-inverting Buck-Boost Converter

The electrical specifications of a non-inverting buck-boost converter are provided in Table 16.2. The overall system block diagram is presented in Figure 16.4, where the error amplifier and PWM generator are achieved by digital components such as DSP chip and user program and PLDs. Basically, the non-inverting buck-boost converter can have three operating modes: buck, boost, and buck-boost. The buck-boost mode is lossy compared to the other modes.

16.1.2.2 Modeling and State Block Diagram of Converter

The electrical specifications are the same as the parameters presented in Table 16.2 and Figure 16.4. The second step is to build the state block diagram of the converter by deriving the system model. Figure 16.5 presents the equivalent circuits of the operating modes in each switching period. The buck operation and boost operation modes do not appear at the same control period. To model the non-inverting buck-boost converter, state space averaging technique [18] is introduced as follows.

For small signal modeling [18],

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Table 16.2 Electrical Specification of Non-inverting Buck-Boost Converter

Input voltage	V_{in} = 4.2 V ~ 2.5 V
Output voltage	V_o = 3.3 V
Inductor	L = 100 uH
Output capacitor	C = 330 uF
Load	R = 4.7 Ω
Switching frequency	f_s = 100 kHz
Minimum effective duty cycle	D_{min_eff} = 6.265%
Maximum effective duty cycle	D_{max_eff} = 98.67%

$$i_L = I_L + \%i_L,\ v_o = V_o + \%v_o,\ v_{in} = V_{in} + \%v_{in},\ \%v_{in} \oplus 0$$

$$d_{buck} = D_{buck} + \%d_{buck} = d_{ctrl} \text{ " } 1,\ d_{boost} = D_{boost} + \%d_{boost} = d_{ctrl} - 1 \geq 0$$

$$d_{buckboost} = D_{buckboost} + \%d_{buckboost} \tag{16.1}$$

For buck operation, the transfer functions and DC gains are

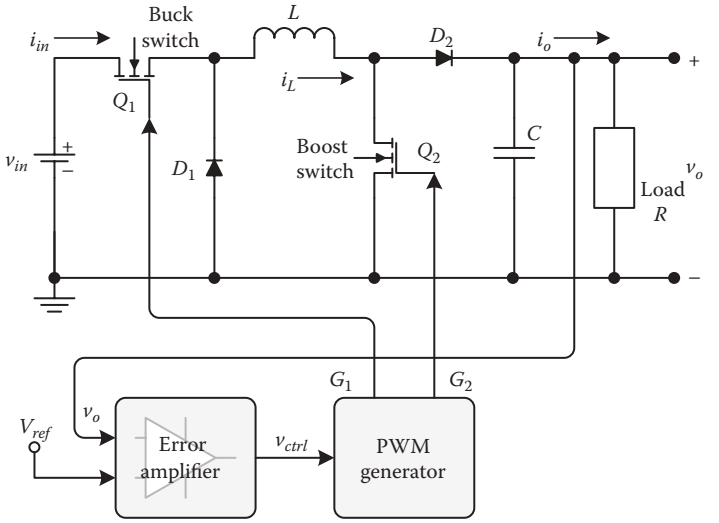
$$\frac{di_L}{dt} = \frac{1}{L}(d_{buck} v_{in} - v_o) \tag{16.2}$$

$$\frac{dv_o}{dt} = \frac{1}{C}(i_L - \frac{v_o}{R}) \tag{16.3}$$

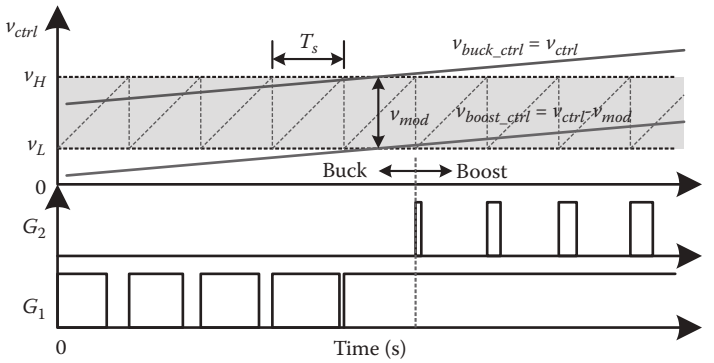
$$\frac{\%v_o(s)}{\%d_{buck}(s)} = \frac{\frac{1}{LC}V_{in}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \quad \text{(small signal model)} \tag{16.4}$$

$$\frac{\%v_o(0)}{\%d_{buck}(0)} = V_{in} \quad \text{(small signal DC-gain)} \tag{16.5}$$

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(a) The Converter



(b) PWM Modulation Strategy (8)

Figure 16.4 Non-inverting buck-boost converter. (a) Converter, (b) PWM modulation strategy [8].

$$V_o(s) = \frac{\frac{1}{LC} V_{in} D_{buck}}{s^2 + \frac{1}{RC} s + \frac{1}{LC}} \quad \text{(large signal model)}, \tag{16.6}$$

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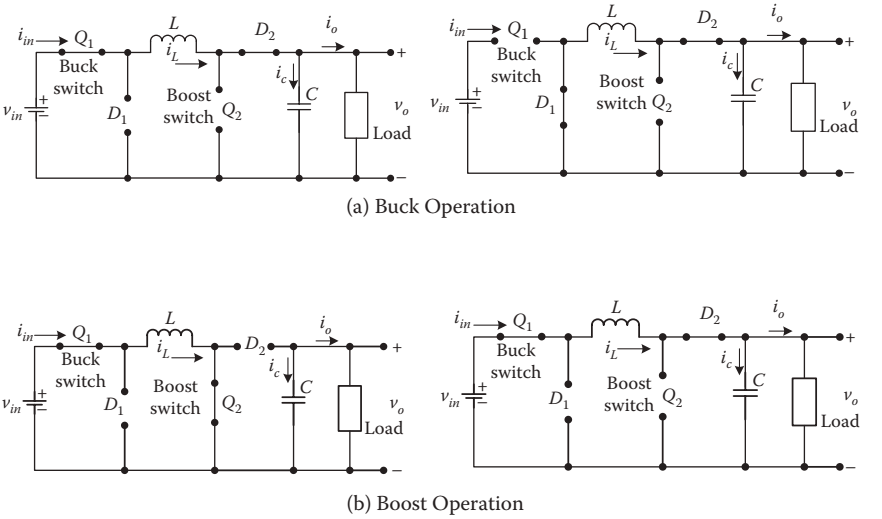


Figure 16.5 Equivalent circuits of operating modes.

$$V_o(0) = V_{in} D_{buck} \quad \text{(large signal DC-gain)} \tag{16.7}$$

For the boost operation, the transfer functions and DC gains are

$$\frac{di_L}{dt} = \frac{1}{L}[v_{in} - (1 - d_{boost})v_o] \tag{16.8}$$

$$\frac{dv_o}{dt} = \frac{1}{C}[(1 - d_{boost})i_L - \frac{v_o}{R}] \tag{16.9}$$

$$\frac{\%v_o(s)}{\%d_{boost}(s)} = \frac{\frac{D'_{boost}}{LC}V_o - \frac{I_L s}{C}}{s^2 + \frac{1}{RC}s + \frac{D'^2_{boost}}{LC}} \tag{16.10}$$

$$\frac{\%v_o(0)}{\%d_{boost}(0)} = \frac{V_o}{D'_{boost}} = \frac{V_o}{1 - D_{boost}} \quad \text{(small signal DC-gain)} \tag{16.11}$$

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$$V_o(s) = \frac{\frac{1}{LC} V_{in}(1 - D_{boost})}{s^2 + \frac{1}{RC}s + \frac{1}{LC}(1 - D_{boost})^2} \quad \text{(large signal model)} \tag{16.12}$$

$$V_o(0) = \frac{V_{in}}{1 - D_{boost}} \quad \text{(large signal DC-gain)} \tag{16.13}$$

The DC gain (steady-state characteristic) of the non-inverting buck-boost converter based on equations (16.1) to (16.13) is plotted in Figure 16.6. In particular, the fact that the steady-state characteristic is continuous in the neighborhood of $d_{ctrl} = 1$ helps designers construct a single controller for the converter with two different operating modes. Even in small signal DC gain in equations (16.5) and (16.11), continuity can be found when $D_{boost} = D_{ctrl} - 1 = 0$.

Figure 16.7 shows the state block diagram constructed based on the state space averaged differential equations (16.2) to (16.9). The converter output voltage can be adjusted by two parameters d_{buck} and d_{boost}. The construction of the state block diagram provides intuitive information about input (feedback) and output signals from the controller. As seen in Figure 16.7, the controller uses v_o and v_{o_ref} as a feedback and the desired output voltage as input signals, respectively. These two signals are processed according to the user procedures as presented in Figure 16.3. The output signals d_{buck} and d_{boost} are given in the form of digital pulse stream, which has a fixed frequency and variable pulse width.

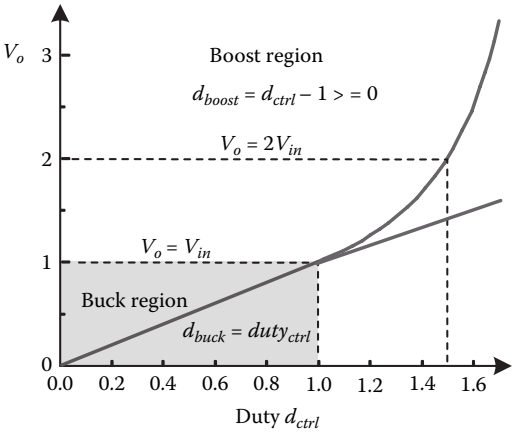


Figure 16.6 DC gain of large signal model.

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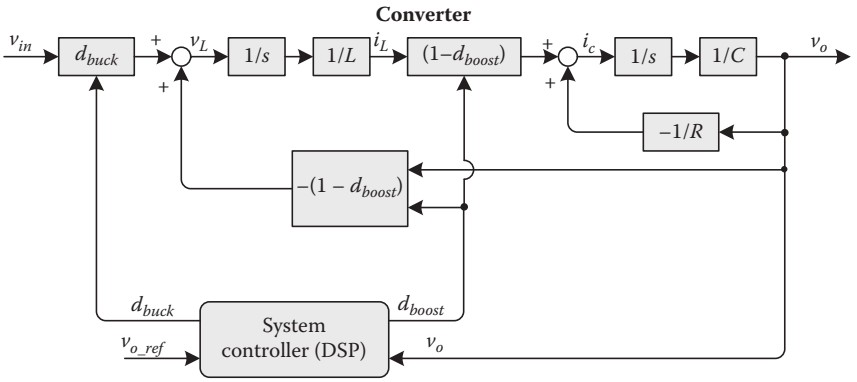


Figure 16.7 State block diagram of system.

16.1.3 Control Flow Based on State Block Diagram

The controller of the system ranges from the traditional PID to the modern techniques such as sliding mode control and adaptive control [19]. The state block diagram provides helpful information in selecting the preferred technique. As an example, a PI controller is introduced in this section.

Figure 16.8 presents the control flow of a classical PI control with anti-windup and the analog implementation of PWM modulation based on Figure 16.4. In the PWM modulator, d_{boost} must be less than one to prevent the inductor current i_L from being extremely high in boost operation mode. In other words, v_{ctrl} is always lower than $2v_{mod}$ as seen in Figure 16.8. The conversion of the control flow into the discrete control follows the control flow diagram. The sampling periods of each control loop, system stability, and control gains can be selected using various discrete control techniques [20].

16.1.4 Selection of DSP and μ-Controller

16.1.4.1 Guidelines for DSP Selection

For proper hardware interface, data types (flags, n-bit integer data, fixed-point data, and floating point data), the necessary hardware architecture, and input/output port should be defined with respect to the system requirements. The DSP chip or μ-controller manufacturers provide the information covering available data types, dedicated multiplier, and built-in internal architectures of their chips. Selection of appropriate DSP chip and μ-controller should consider the following criteria:

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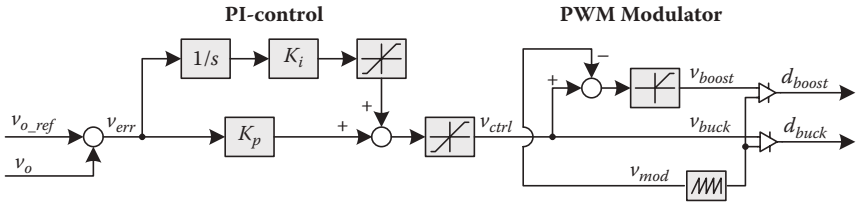


Figure 16.8 Control flow diagram.

1. Build an input/output signal specification table.
   - How many inputs and outputs are necessary?
   - Are the signals analog or digital (ADC/DAC/digital IO ports)?
   - What are the feasible voltage and current ranges of each input and output port?
2. What and how many operations/calculations does your controller need?
   - Integer/fixed point/floating point operations/calculations (8 bit, 16 bit, 32 bit, and 64 bit) based on your control routines.
3. How many "millions of instruction per second" (MIPS) are available from the DSP?
   - The faster (shorter) control period your system requires, the higher MIPS is necessary on the average. (It is recommended to track the number of instructions performed within that control period.)
   - Available MIPS generally tends to be increased by available clock speed (dependent on crystals and/or oscillators) of the DSP chips.
4. How much and what types of memory are available (size and types of data and program memory; Figure 16.9)?
5. What specific/special functions does your system require from the DSP chip?
   - Timer/counter, external interrupt request, analog-to-digital converter, digital-to-analog converter, up/down counter for two-phase incremental encoder signal, symmetric space vector PWM output for motor control, communication protocol (asynchronous/synchronous, CAN, I^2C, TCP/IP, etc.), program downloading (via JTAG, RS-232, and so on).
6. Other requirements (cost, physical dimension, soldering conditions, etc.)?

16.1.4.2 Selection of DSP Chip

We now consider estimation of operation/calculation load and data types. Based on the control flow diagram in Figure 16.8, the difference equations for DSP can be derived as

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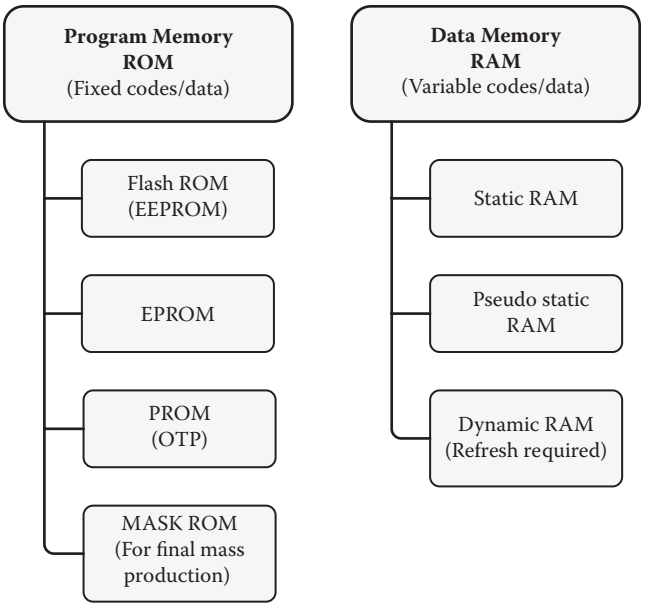


Figure 16.9 General criteria of memory types.

$$v_{err}[kT_s] = v_{o\_ref}[kT_s] - v_o[kT_s] \tag{16.14}$$

$$v_{ctrl}[(k+1)T_s] = K_p v_{err}[kT_s] + K_i \sum_{n=0}^{k} v_{err}[nT_s] \tag{16.15}$$

$$v_{ctrl}[(k+1)T_s] \le V_{ctrl\_\max} \tag{16.16}$$

$$v_{buck}[(k+1)T_s] = v_{ctrl}[(k+1)T_s] \qquad 0 \le v_{buck}[(k+1)T_s] \le 1 \tag{16.17}$$

$$v_{boost}[(k+1)T_s] = v_{ctrl}[(k+1)T_s] - V_{\mathrm{mod}} \qquad 0 \le v_{boost}[(k+1)T_s] < 1 \tag{16.18}$$

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$$d_{buck}[(k+1)T_s] = \frac{v_{buck}[(k+1)T_s]}{V_{\text{mod}}} \tag{16.19}$$

$$d_{boost}[(k+1)T_s] = \frac{v_{boost}[(k+1)T_s]}{V_{\text{mod}}} \tag{16.20}$$

where $v_{o\_ref}[kT_s]$, $v_o[kT_s]$, K_p, K_i, and T_s are the sampled output reference voltage, output voltage, proportional gain, integral gain, and sampling period, respectively. Equations (16.14) to (16.20) are performed in every sampling/control period (set by timer interrupt request) by the DSP or µ-controller.

Based on the electrical specification in Table 16.2, the switching frequency f_s is 100 kHz, which means T_s = 10 µs. In other words, the operations/calculations and comparisons for discrete control routine must be able to be completed within 10 µs. However, the execution time should not exceed the half sampling period, since the subroutines in the user program have to be executed during the idling time of control routines. As a result, the total execution time of a control routine must be shorter than 5 µs. If the type of data is 16-bit integer then the DSP should be able to perform 16 × 16 multiplication and 32/16 division by using either the dedicated architecture or software library. In the case that either the fixed or floating point data are required, the DSP should have capabilities in the fixed/floating point multiplication and divisions through the specialized arithmetic units or software library.

Through the manufacturers' specification tables, many different DSP chips can be chosen. For the example of non-inverting buck-boost converter, TMS320F2812 by Texas Instruments has been chosen. TMS320F2812 has 150 MIPS, which would be enough for the discrete control of the motor drive, inverter, and converter. TMS320F2812 has a dedicated multiplier inside the chip and provides the library for floating point operation. Also, the furnished flash read-only memory (ROM) for program memory gives a chance for the user to revise the system program easily.

16.1.5 Detailed Datasheets and Manuals

In order to properly utilize the selected DSP or µ-controller, the designer needs to gather the detail electrical datasheet, various application notes, and manuals regarding the software development environment. First of all, a good understanding of the internal architecture and electrical specification of the DSP is very important for the system hardware designing and for the software development.

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In order to properly use a DSP chip, the designer needs several materials explaining

- Internal hardware and electrical specification of DSP chips
- Using the compiler/linker to generate user program code (assuming compiler/linker/unified software development environment is provided)
- Downloading or writing code to the DSP chip (assuming downloading tools are provided)
- Initializing and utilizing internal peripherals of DSP using software
- Changing the booting mode when power is on
- Using a starter-kit for beginners (easier way to approach the DSP chip)
- Application notes associated with users' applications

The designer should be familiar with C/C++ languages or assembly languages compatible with the selected DSP chip.

16.1.5.1 Internal Architecture and Electric Specifications

The data manual includes overall and detail information on the DSP chip. Figure 16.10 shows the architecture of the selected DSP chip. For the TMS320F2812 chip, the manufacturer provides the literature SPRS174M, which is named *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 Digital Signal Processors Data Manual*. Using this material, the designer can find what internal hardware function is available and which more detailed manual is necessary.

Table 16.3 presents several materials related to TSM320F2812 hardware. The shaded materials are recommended to read for the implementation of a digital controller of a non-inverting buck-boost converter. The designer can easily find this literature on the Texas Instruments Web site.

16.1.5.2 Software Development Environment (Assembler, Compiler, Linker, and Downloader)

With the hardware manuals of the selected DSP chip or μ-controller, the designer should have enough materials explaining the software development environment. As a rule, these materials consist of the assembler, compiler, linker, program downloader, and the unified development tool manuals. The unified development tool helps the user perform all the processes to generate from the source codes to the final execution codes. In the case of the Texas Instruments DSP products, the manufacturer

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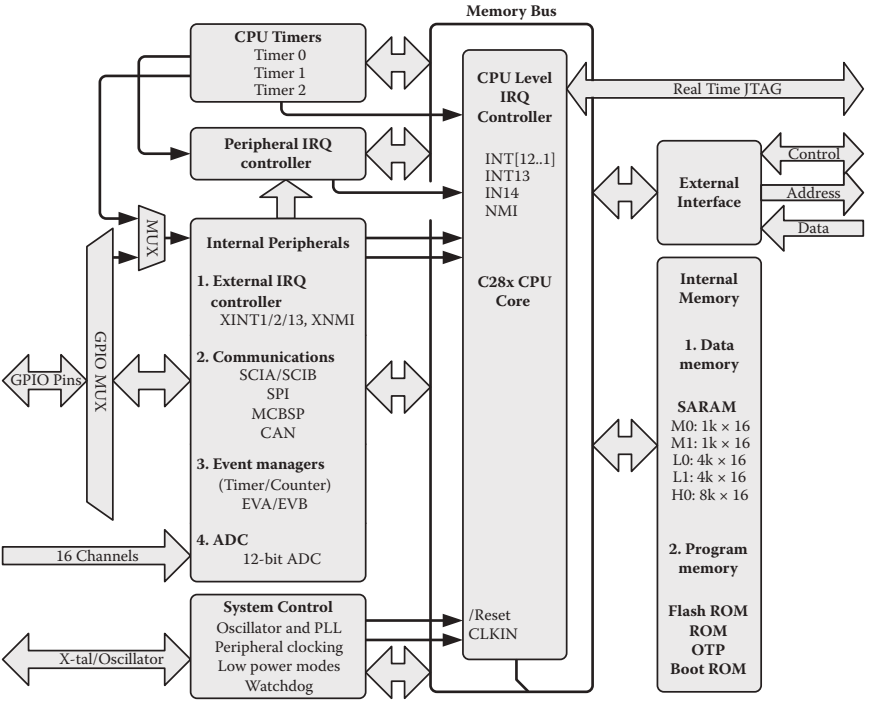


Figure 16.10 Overall internal architecture of TMS320F281x DSP.

supplies the unified tools in its Code Composer Studio (CCS). Even though the designer develops the software for the DSP chip on the basis of the unified tools, it is still recommended for the designer to have enough knowledge of the assembler, compiler, linker, and program downloader manuals. Figure 16.11 presents the software development flow based on CCS. This flow is also similar to other unified development tools provided by different DSP chip manufacturers. Table 16.4 lists the materials to be consulted.

16.1.5.3 Commercial DSP Starter Kit

The commercial DSP starter kit is very useful in providing required information for beginners. The kit provides a DSP board on which various test pins/ports are available for the user to get basic experience in handling and understanding of the selected DSP's functions. Most beginners would be advised to utilize the starter kit and implement several functional requirements. Designing and building custom DSP boards based on system requirements is very useful; however, the processes require experience. Various starter kits are available, depending on the provided

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Table 16.3 Materials Related to TMS320F1812 Hardware

Title	Literature No.
TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 Digital Signal Processors Data Manual	SPRS174M
TMS320x28xx, 28xxx DSP Peripheral Reference guide (Rev. F)	SPRU566F
TMS320x281x System Control and Interrupts Reference Guide (Rev. E)	SPRU078E
TMS320x281x Multichannel Buffered Serial Port (McBSP) Reference Guide (Rev. C)	SPRU061C
TMS320x281x Event Manger (EV) Reference Guide (Rev. E)	SPRU065E
TMS320x281x, 28xxx Serial Peripheral Interface (SPI) Reference Guide (Rev. D)	SPRU059D
TMS320x28xx, 28xxx Enhanced Controller Area Network (eCAN) Reference Guide (Rev. E)	SPRU074E
TMS320x281x Analog-to-Digital Converter (ADC) Reference Guide (Rev. D)	SPRU060D
F2810, F2811, and F2812 ADC Calibration	SPRA989A
TMS320x28xx, 28xxx Serial Communication Interface (SCI) Reference Guide (Rev. B)	SPRU051B
TMS320x28x DSP CPU and Instruction Set Reference Guide (Rev. D)	SPRU430D
TMS320x281x Boost ROM Reference Guide (Rev. C)	SPRU095C
TMS320x281x External Interface (XINTF) Reference Guide (Rev. C)	SPRU067C

Source: Texas Instruments. 2008. Technical documents: C2000TM high performance 32-bit controllers—tools user guide. http://focus.ti.com/dsp/docs/dspsupporttechdocs.tsp?sectionId=3&tabId=409&techDoc=6&familyId=1406&documentCategoryId=6&toolTypeId=0&viewType=0&toolTypeFlagId=2.

functions, cost, and downloading tools. Texas Instruments provides the information of starter kits [23].

16.1.5.4 Application Notes

Based on the selected DSP chip or μ-controller, the manufacturers provide a wide range of application notes to promote the sale of their products [24]. The application notes cover fields such as motor control, communication, image processing, inverter/converter control, temperature control, battery charger, automotive systems, display device control, and numerous other applications. Usually, a user is able to find the applicable notes on the chip manufacturer's Web site. The exact application and technique might be different. Nevertheless, the application notes will provide the user with helpful information.

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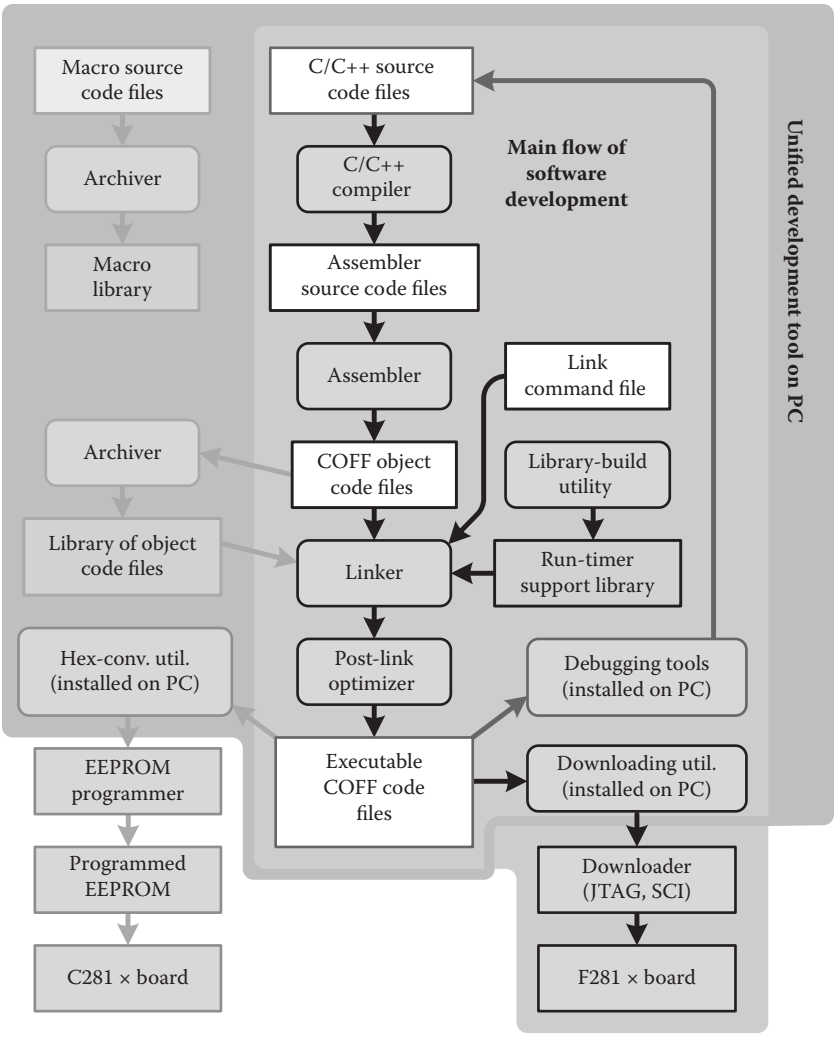


Figure 16.11 Overall internal architecture of TMS320F281x DSP.

16.2 Hardware Schematic Design of Non-inverting Buck-Boost Converter and DSP Control Board

In this section, actual circuit diagrams and their explanations are presented for the purpose of PCB implementation. It is assumed that the designer has proper knowledge of the selected DSP chip and software development environment. In addition, the designer has enough knowledge of control

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Table 16.4 Materials Associated with Software Development Environment [22]

Title	Literature No.
Code Composer Studio Development Tools v.3.1 Getting Started Guide (Rev. H)	SPRU509H
TMS320C28x Optimizing C/C++ Compiler User's Guide (Rev. C)	SPRU514C
TMS320C28x Assembly Language Tools User's Guide (Rev. C)	SPRU513C
TMS320F29xx SDFlash Serial RS232 Flash Programming Reference Guide	
IQmath Library (A Virtual Floating Point Engine) Module User's Guide	

object and control scheme. The circuit diagrams show the non-inverting buck-boost converter and the connectivity between the DSP chip and external circuits. The external circuits include the analog signal interface, digital signal interface, low-voltage power circuit, booting mode selecting circuit, RS-232 serial communication circuit, serial D/A converter, serial EEPROM, and JTAG interface circuit.

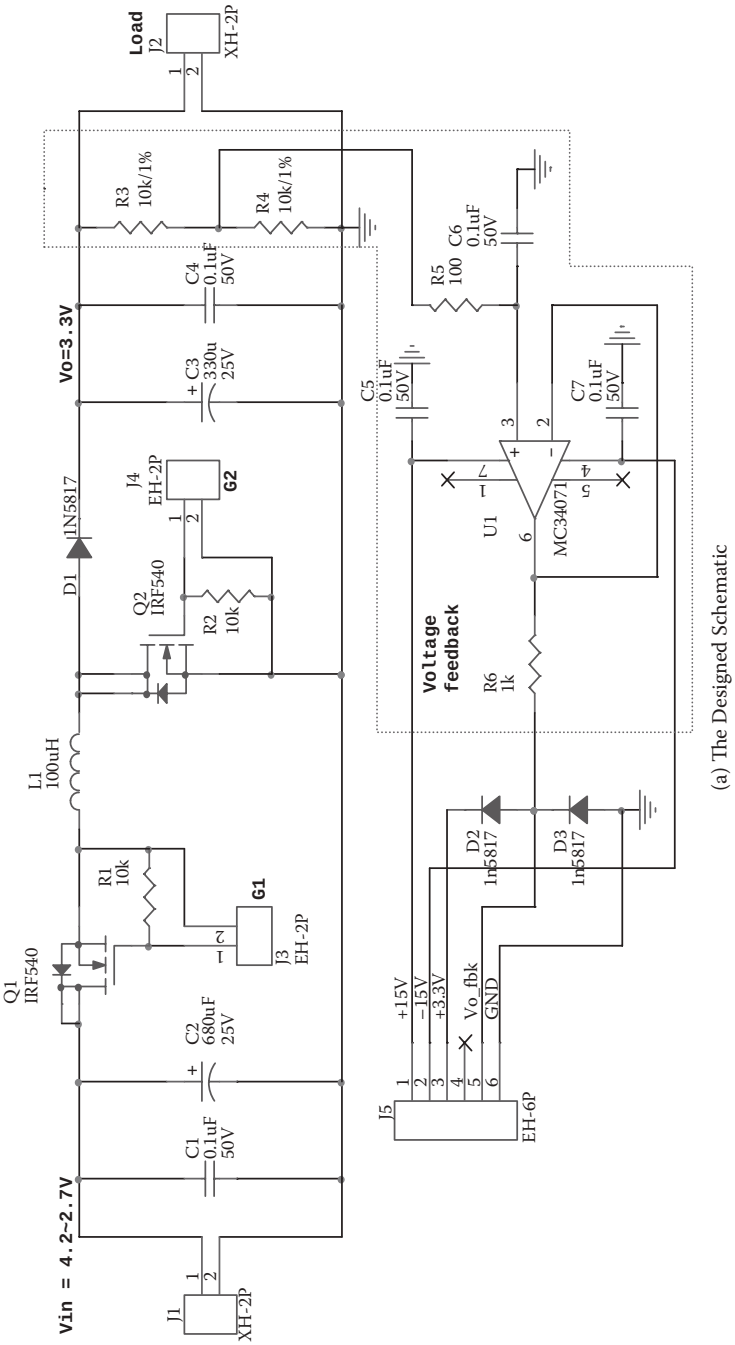
16.2.1 *Schematic for Non-inverting Buck-Boost Converter*

The beginning of design of a DSP chip or μ-controller is to draw schematics of the object to be controlled. Thus, the schematic is derived from Figures 16.4 and 16.5. The selection of components such as switches, diodes, resistors, inductors, and capacitors are based on the designer's preferences and circuit parameters [18]. For real component selection, the designer needs various component parameters such as the range of operating voltage/current/power, heat radiation, frequency characteristics, switching time, parasitic RLC values, and costs. In the provided schematics, all of the parameters have been based on the author's preferences. Figure 16.12 presents the schematic of the non-inverting buck-boost converter where G_1, G_2, v_{in}, v_o, and v_{o_fbk} are identified as the buck switch gate signal, boost switch gate signal, converter input voltage, output voltage, and output voltage feedback signal, respectively. The circuit is only for explanation purposes.

16.2.2 *Selected DSP Chip Connectivity*

Figure 16.13 shows TMS320F2812 DSP chip connectivity. The electrical specification of the chip datasheet or manual must be carefully reviewed so that proper signal exchanges are kept within the maximum electrical ratings.

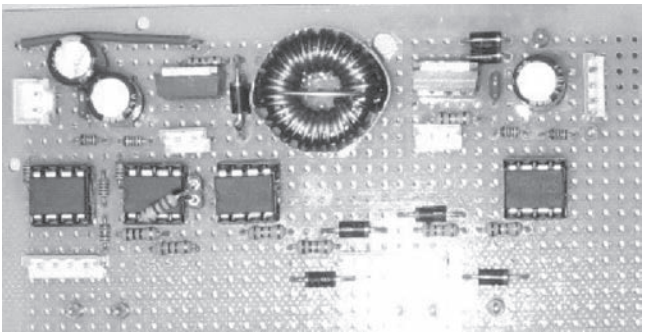
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(a) The Designed Schematic

Figure 16.12 Non-inverting buck-boost converter.

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(b) The Built Converter

Figure 16.12 (continued)

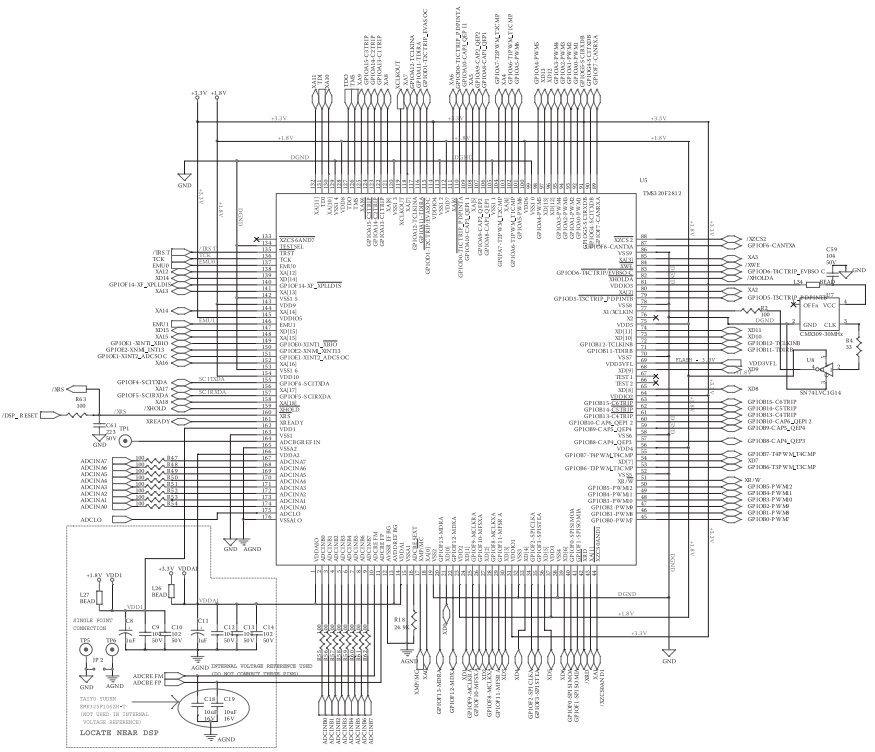


Figure 16.13 TMS320F2812 DSP chip connectivity.

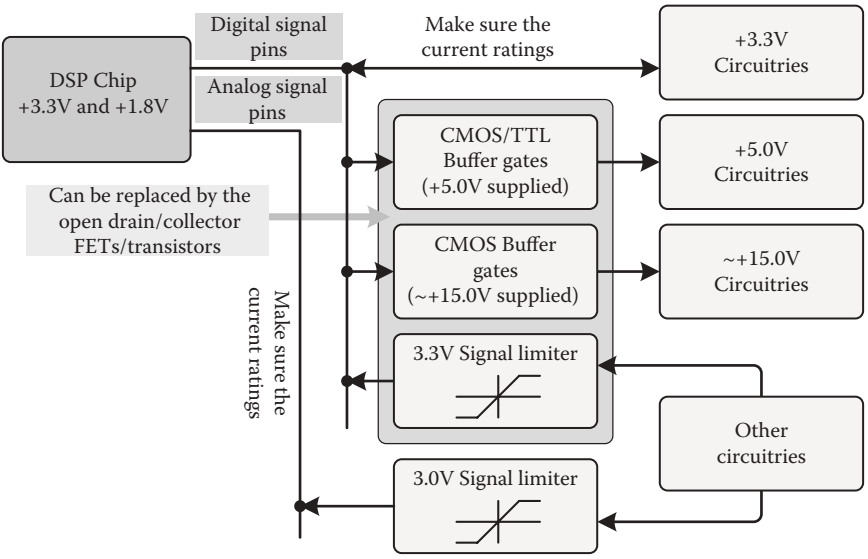
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16.2.3 Analog and Digital Signal Interface

Figure 16.14 provides the interface circuits between DSP and the external digital/analog signals. The external digital/analog signals are composed of gating PWM signals, gating logic control signals, output voltage feedback signal, and low voltage power lines. Through the filtering functions of these circuits, the DSP chip is protected from the line electromagnetic interference (Line EMI) and voltage/current surges.

16.2.4 Low Voltage Power and DSP Chip Reset Circuit

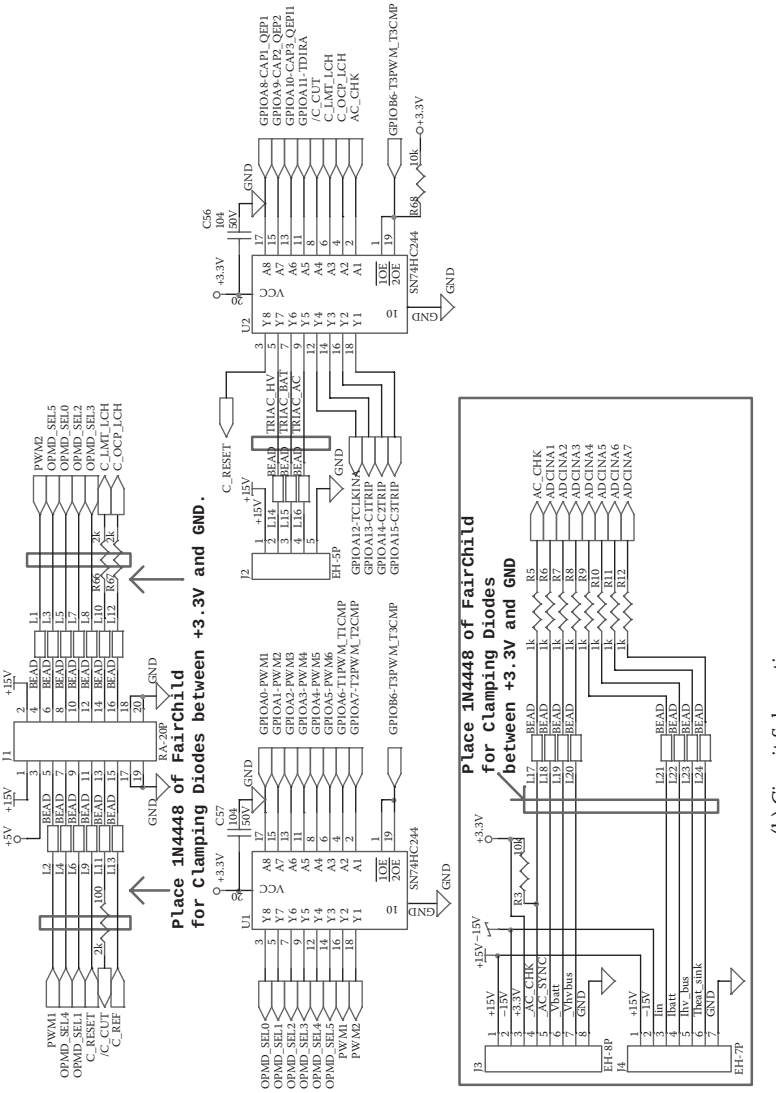
Figure 16.15 is the circuit to power the DSP control board and auxiliary power for the non-inverting buck-boost converter. The supplied voltages are +15 V, –15 V, +5 V, +3.3 V, and +1.8 V where +15 V, –15 V, and +5 V have another purpose: to interface with external circuitries such as the analog amplifier, current sensors, MOSFETs, transistors, and TTL/CMOS components. Figure 16.15a is the circuit for +15 V, –15 V, and +5 V supply. Figure 16.15b shows the +3.3 V and +1.8 V circuit to power the DSP chip. Along with designing hardware schematics, the designer needs to complete voltage maps depicting the power line connections in the hardware



(a) An Electrical Signal Interface Diagram Between DSP Chip and External Circuitries

Figure 16.14 Digital/analog signal interface. (a) An electrical signal interface diagram between DSP chip and external circuitries, (b) circuit schematic.

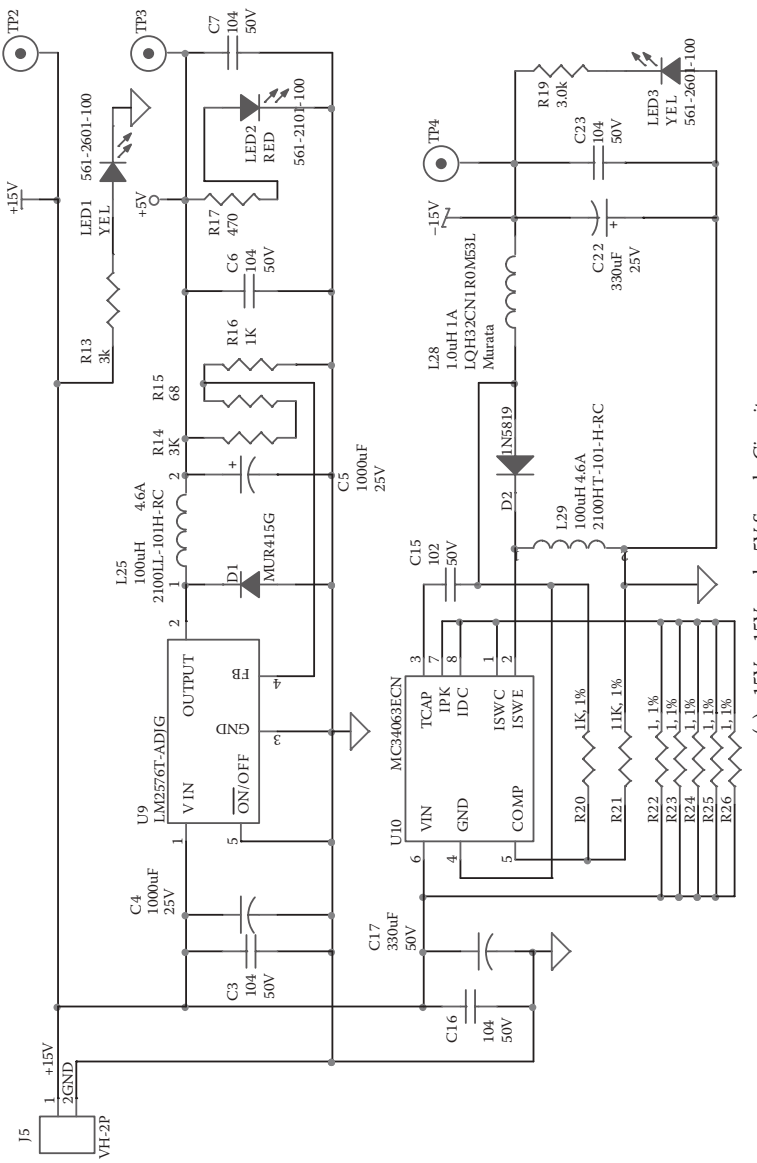
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(b) Circuit Schematic

Figure 16.14 (continued)

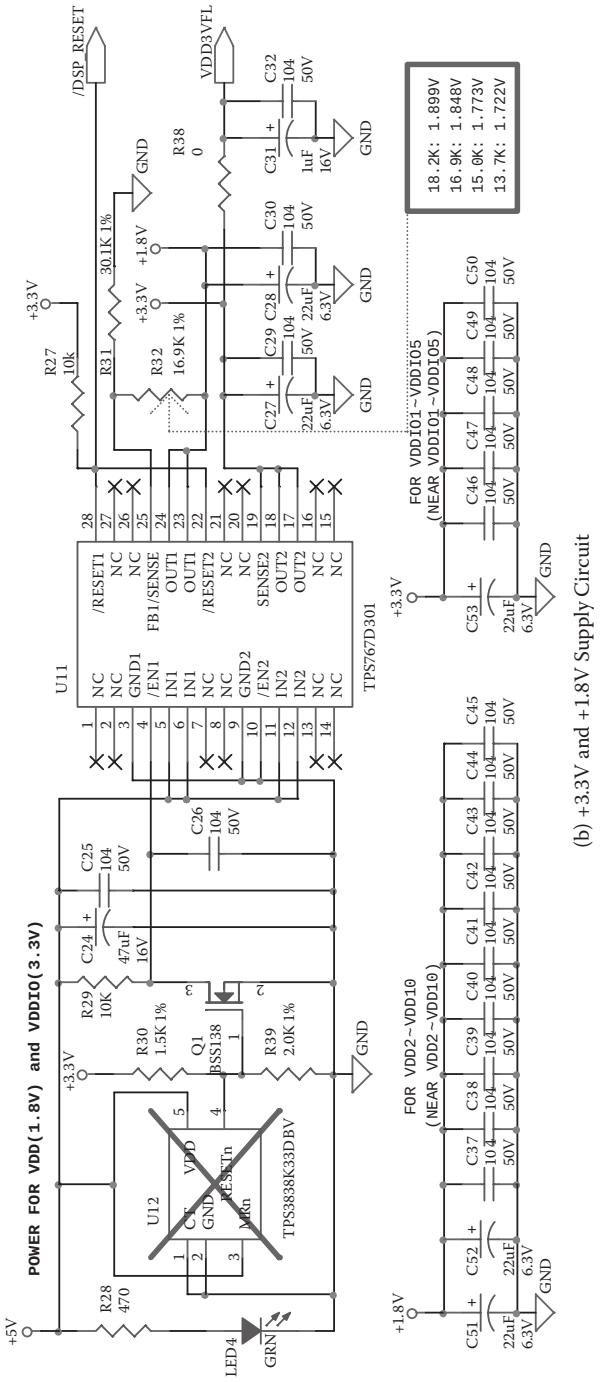
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(a) +15V, –15V, and +5V Supply Circuit

Figure 16.15 Low voltage supply circuits. (a) +15 V, –15 V, and +5 V supply circuits, (b) +3.3 V and +1.8 V supply circuits.

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(b) +3.3V and +1.8V Supply Circuit

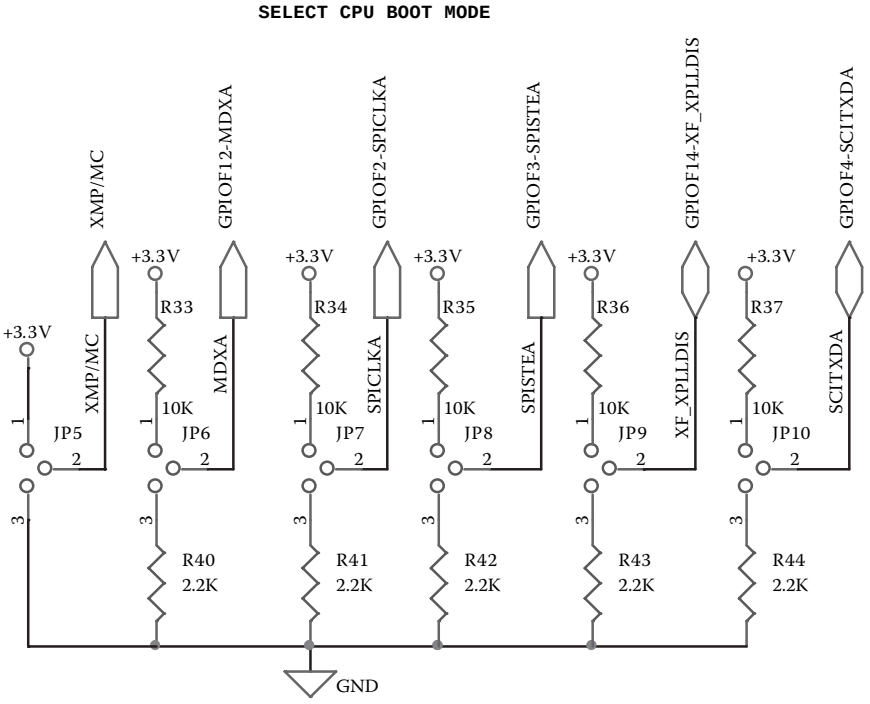
Figure 16.15 (continued)

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schematic. On the basis of voltage maps, the circuit is divided into several parts and the interface is clarified.

16.2.5 Boot Mode Selecting Circuit

The boot mode selecting circuit is used to set the DSP's operations right after power is on (Figure 16.16). The operations include μ-processor or μ-controller mode selection, PLL mode selection, and booting code operation. The μ-processor mode/μ-controller mode is used to determine the use of internal program memory. Through utilizing the boot code, the programmer selects the execution media of user boot code and user program. The execution media are SPI, SCI, parallel I/O port, H0 SARAM, flash ROM, and OTP ROM. The details are found in references [25] and [26].



(a) Booting mode selecting circuit

Figure 16.16 Boot mode selection.

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MODE	SCITXDA	MDXA	SPISTEA	SPICLKA
Flash	1	X	X	X
SPI	0	1	X	X
SCI	0	0	1	1
HO	0	0	1	0
OTP	0	0	0	1
Parallel	0	0	0	0

PLL Enable/Disable	
Disable	XF_XPLLDIS=0
Enable	XF_XPLLDIS=1

μ-Processor / μ-Controller	
μ-Processor	XMP/MC=1
μ-Controller	XMP/MC=0

(b) Booting mode selecting table

Figure 16.16 (continued)

16.2.6 *RS-232 Serial Communication Circuit*

The asynchronous serial communication based on the RS-232 protocol is one of the helpful ways to transfer data between digital devices, although the communication speed is relatively slower than other up-to-date communication protocols. However, asynchronous communication using RS-232 is still widely used in many applications because of the easy implementation. In this chapter, the RS-232 serial communication is used for monitoring the internal operations of user program, which is a very useful technique to debug the user program, even when taking advantage of the processor emulators. Figure 16.17 presents the schematic of RS-232 communication for TSM320x281x DSP chips.

16.2.7 *Serial Interface with D/A Converter, EEPROM, and JTAG Port*

A digital-to-analog converter (DAC) is used to convert the digital operation results into analog signals, which is a final process of digital signal processing. In addition, DAC is useful in monitoring the internal calculation results in almost real time. The software developer is able to trace the calculation results from control routines by watching the oscilloscope. In order to store user parameters in the control system, EEPROMs are frequently used. When internal EEPROM is not available, the designer adds external EEPROMs to DSP chips or μ-controllers. Introducing DAC and EEPROM

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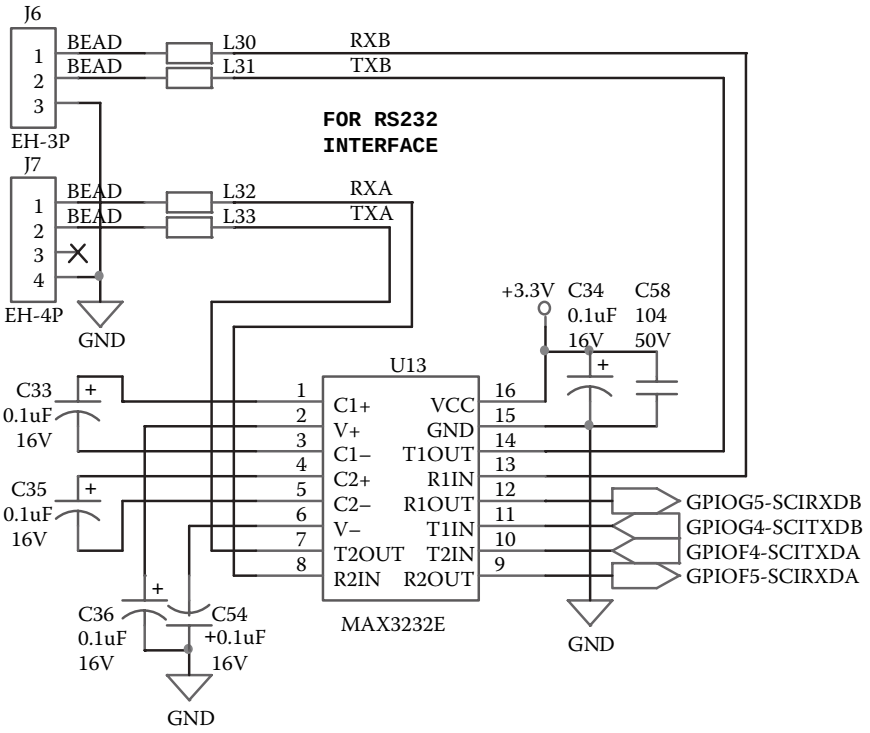


Figure 16.17 RS-232 communication circuit.

with serial interfaces reduces the number of wires in connecting DSP chips with external devices. Many DSP chip or µ-controller programmers use the JTAG port to download and emulate the user program on the basis of the boundary scan technology. For a software developer's convenience, many DSP chip and µ-controller manufacturers provide a JTAG port on their products as well as a JTAG downloader and emulator. Figure 16.18 shows the schematic for serial interface of DAC, EEPROM, and JTAG.

Figure 16.19 shows the self-designed digital controller PCB using the schematics from Figures 16.13 to 16.18.

16.3 Software Implementation for Control System

16.3.1 Defining Program Module Diagram According to Functionalities (or Tasks)

The basic structure for implementing the functional requirements into user programs is as shown in Figure 16.2. The designer divides the whole

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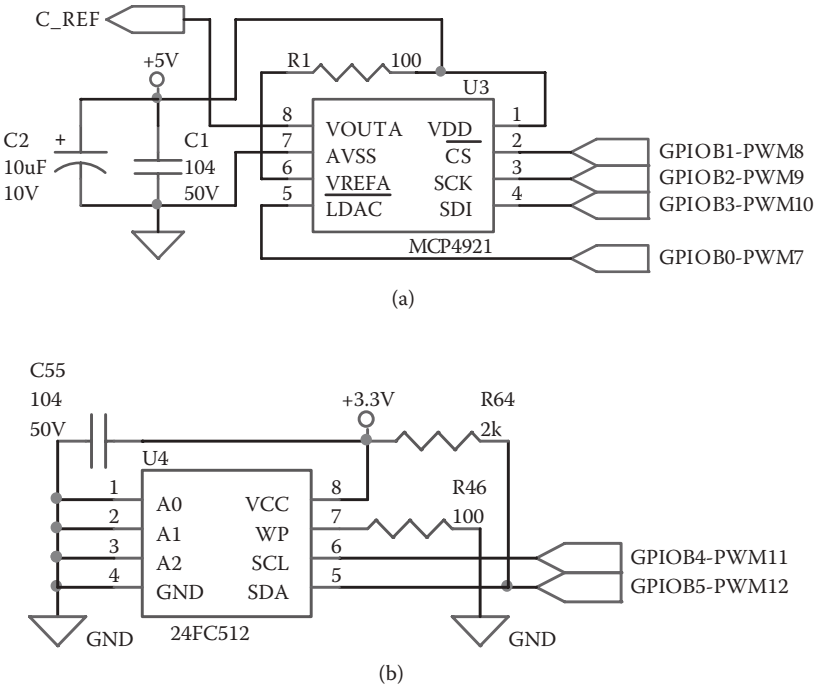


Figure 16.18 Serial interface with DAC, EEPROM, and JTAG port. (a) Serial DAC, (b) serial EEPROM, (c) TAG Port..

software into several modules according to the functional requirements (or tasks). Figure 16.20 provides the software module diagram for the control of a non-inverting buck-boost converter. As mentioned earlier, the designer needs to be familiar with C/C++ programming language and the materials associated with software development environment in Table 16.4. It will also be useful to download and use the fundamental source codes such as the start-up code file, link command file, and header files for the DSP's internal peripherals.

16.3.2 Link Command File

In Figure 16.11, the linker on software development flow links all the object code modules into one executable file based on the information given by the user. The linking information is described in the link command file, which defines the sizes and positions of program/data memory. For details, see Reference 22. Figure 16.21 presents a part of the link command file on the unified development tools.

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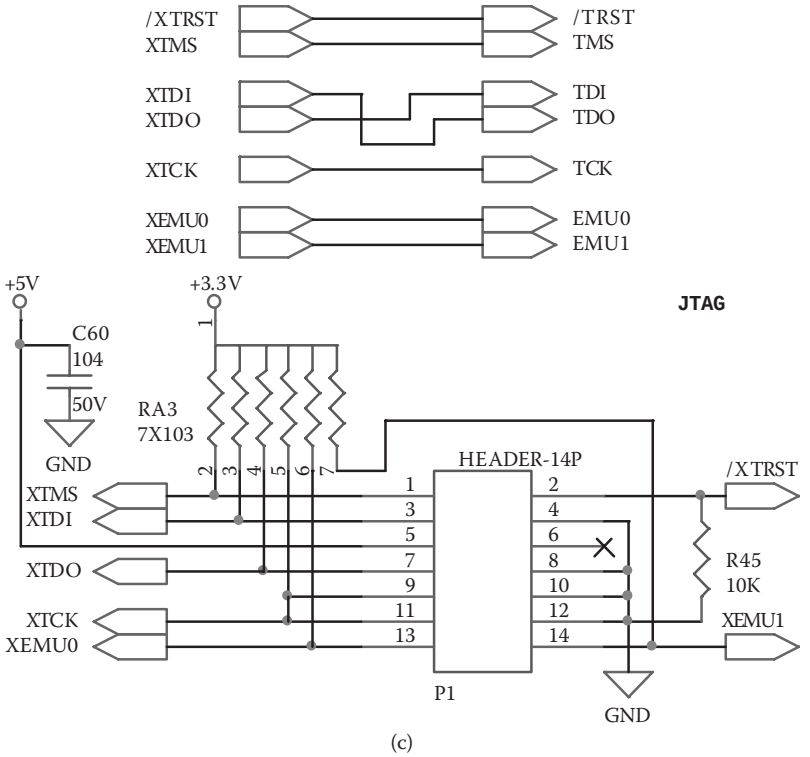


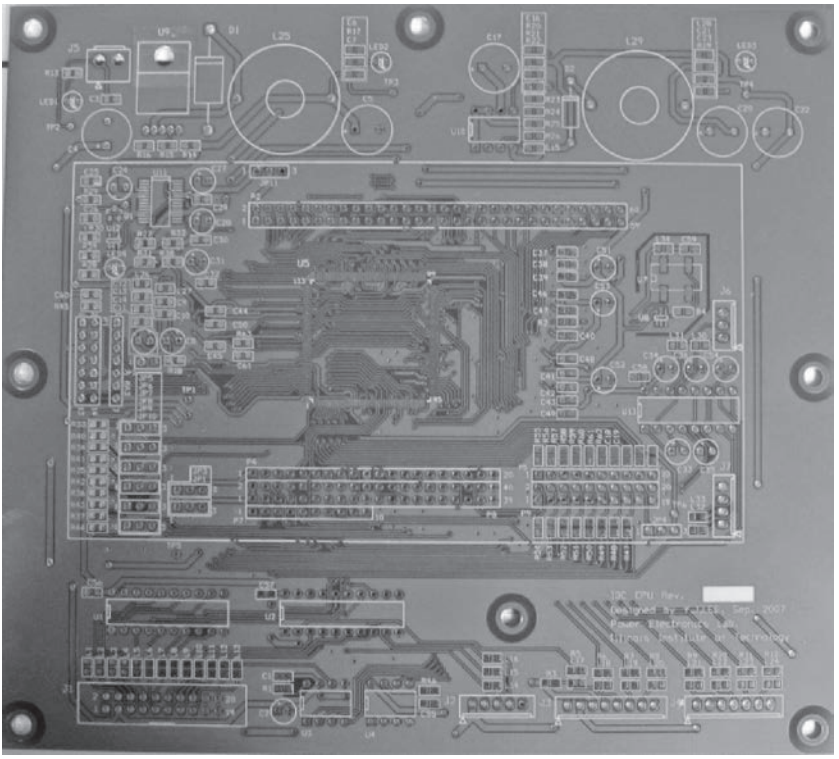
Figure 16.18 (continued)

16.3.3 Start-up Code

The start-up code is an assembly language program that prepares for an execution of C/C++ language code. The linker links the start-up code into the executable code file and then the start-up code is executed first when the user program runs on the DSP chip.

The start-up code performs several initializations for internal peripherals, data memory, and interrupt vectors/handlers, and then "jumps or calls" the initial function such as "main( )" on the run-time library or user program. The initial function is a program start point at the user-level C/C++ program. In many cases, the start-up code is provided by the software tool suppliers. Programmers might or might not make minor changes on the start-up code for the applications. Once the start-up code is fixed, programmers only have to develop user application code at the C/C++ level. Figure 16.22 presents an example of the start-up code.

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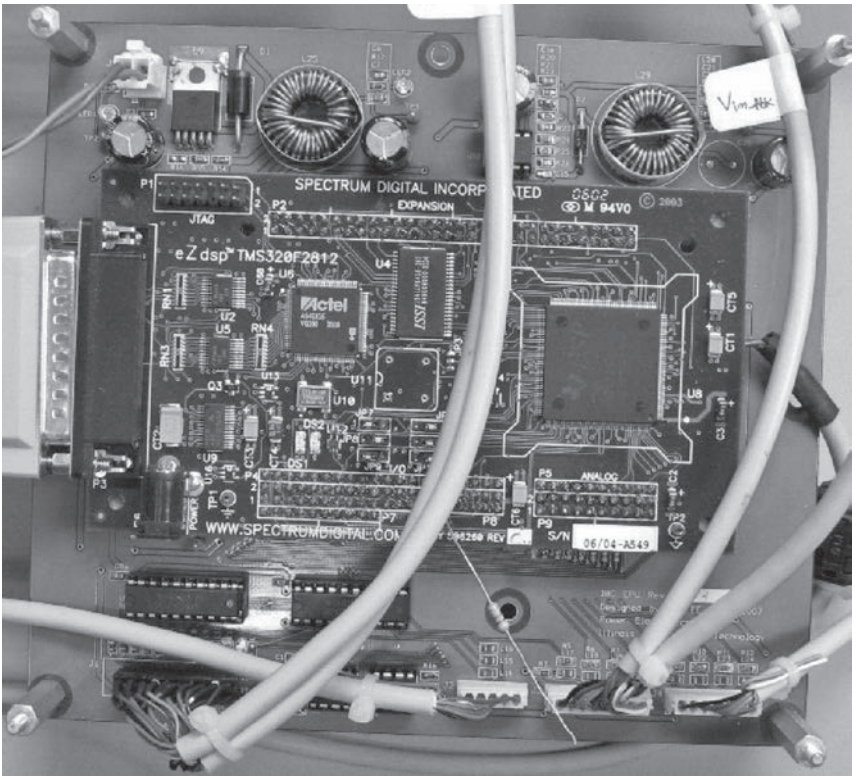
(a)

Figure 16.19 (a) Self-designed digital controller PCB, (b) completed controller combined with starter kit.

16.3.4 *Header Files and Module to Define Special Function Registers*

As seen in Figure 16.10, the internal architecture of a DSP chip or µ-controller has special function registers corresponding to the peripheral devices such as ADCs, timers/counters, digital I/O ports, communication ports, interrupt service request masks, etc. Special function registers (SFRs) specify or determine the detail operations of internal peripheral devices. Therefore, whenever setting up internal peripherals is necessary, programmers look up the hardware manual [21], [26] in order to have the specifications of SFRs to use. For a programmer's convenience, the software development tool providers supply several header files and C/C++ code files, which define the SFRs. The programmers only include, compile,

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(b)

Figure 16.19 (continued)

and link these files with other modules. Whenever access to some SFRs is required, simply assigning values to the SFRs is enough to set up the corresponding peripheral devices. Figure 16.23 presents the files listed on the software development project where DSP281x_xxxxxxxxx.h and SFR.C files contain the definitions of SFRs.

16.3.5 Construction of Control Flow Chart for Controller

The preparatory files such as the link command file, start-up code file, and SFR-related files have been overviewed. In parallel with understanding of the preparatory files, the programmer needs to build the control flow chart based on the actual modules and function names. As shown in Figure 16.3, the digital signal processing with DSPs or μ-controllers is

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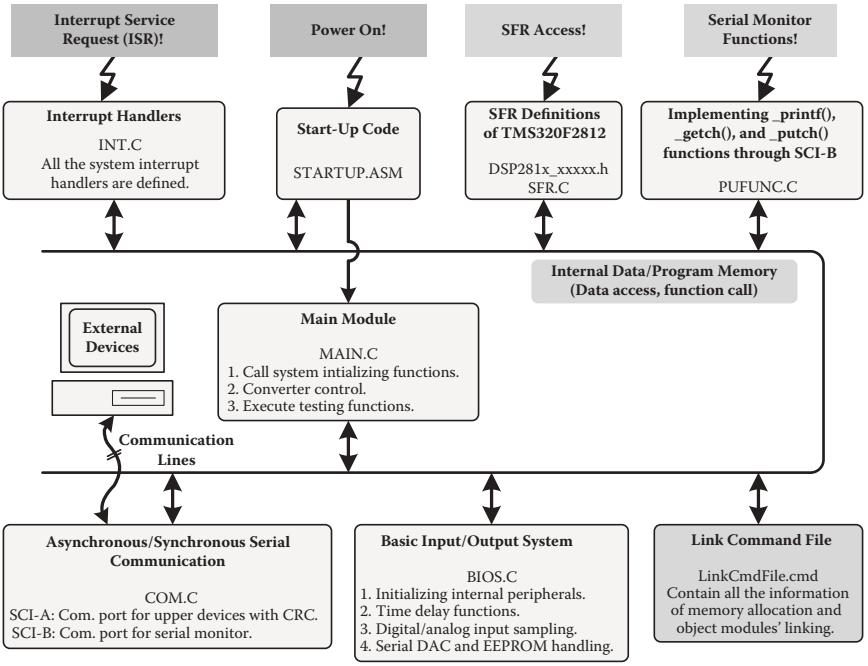


Figure 16.20 Modular diagram of source codes.

based on the periodic execution of control routine by timer interrupt service request. Time interval (or sampling time) is established by assigning a proper counting value to the timer/counter-related SFRs and by enabling the operation of timer/counter and interrupt request handling. The materials [26]–[28] are helpful in setting the internal timers/counters of TMS320F2812. Figure 16.24 provides an example of the flow chart to construct the control routines of the user program.

16.3.6 Composing Source Codes for Non-inverting Buck-Boost Converter

For the understanding of the flow chart in Figure 16.24, this section presents main routines of several files shown in Figures 16.20 and 16.23, which are BIOS.C, COM.C, INT.C MAIN.C, and PUFUNC.C. These routines are only examples of composing source codes which depend on the preference of the programmer. Also, Texas Instruments provides many programming examples with regard to the internal peripherals and applications that a programmer can consult.

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LinkCmdFile.cmd

```
-c
-stack 0x400        /* 1024[words] : STACK size allocated to
-heap  0x200        /*  512[words] : HEAP  size allocated to


MEMORY
{
PAGE 0:
     /*** Program Memory ***/
     FLASH(RX)      : origin = 0x3D8000, length = 0x01FF80
     CSM_RSVD(R)    : origin = 0x3F7F80, length = 0x000076
     FLASHBOOT(RX)  : origin = 0x3F7FF6, length = 0x000002
     PASSWORDS(R)   : origin = 0x3F7FF8, length = 0x000008
     BOOTROM(RX)    : origin = 0x3FF000, length = 0x000FC0
     BRROMVECT(R)   : origin = 0x3FFFC0, length = 0x000040

PAGE 1:
     /*** Data Memory ***/
     M0RAMVECT(RW)  : origin = 0x000000, length = 0x000040
     M0M1RAM(RW)    : origin = 0x000040, length = 0x000800
     L0L1RAM(RW)    : origin = 0x008000, length = 0x002000
     H0RAM(RWX)     : origin = 0x3F8000, length = 0x002000

     /*** Peripheral Register Files ***/
     DEV_EMU(RW)    : origin = 0x000880, length = 0x000180
     PIE_VECT(RW)   : origin = 0x000D00, length = 0x000100
     FLASH_REGS(RW) : origin = 0x000A80, length = 0x000060
     CSM(RW)        : origin = 0x000AE0, length = 0x000010
     XINTF(RW)      : origin = 0x000B20, length = 0x000020
     CPU_TIMER0(RW) : origin = 0x000C00, length = 0x000008
     CPU_TIMER1(RW) : origin = 0x000C08, length = 0x000008
     CPU_TIMER2(RW) : origin = 0x000C10, length = 0x000008
     PIE_CTRL(RW)   : origin = 0x000CE0, length = 0x000020
     ECANA(RW)      : origin = 0x006000, length = 0x000040
     ECANA_LAM(RW)  : origin = 0x006040, length = 0x000040
     ECANA_MOTS(RW) : origin = 0x006080, length = 0x000040
     ECANA_MOTO(RW) : origin = 0x0060C0, length = 0x000040
     ECANA_MBOX(RW) : origin = 0x006100, length = 0x000100
     SYSTEM(RW)     : origin = 0x007010, length = 0x000020
     SPIA(RW)       : origin = 0x007040, length = 0x000010
     SCIA(RW)       : origin = 0x007050, length = 0x000010
     XINTRUPT(RW)   : origin = 0x007070, length = 0x000010
     GPIOMUX(RW)    : origin = 0x0070C0, length = 0x000020
     GPIODAT(RW)    : origin = 0x0070E0, length = 0x000020
     ADC(RW)        : origin = 0x007100, length = 0x000020
     EVA(RW)        : origin = 0x007400, length = 0x000040
     EVB(RW)        : origin = 0x007500, length = 0x000040
     SCIB(RW)       : origin = 0x007750, length = 0x000010
```

Figure 16.21 Link command file.

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STARTUP.ASM

```
JTAGRTDX        .set    1               ;JTAG RTDX enabled
WD_DISABLE      .set    1               ;set watchdog timer disabled

        .def    RESETIV                 ;define   RESETIV
        .def    RESET_ISR               ;define   RESET_ISR
        .def    NULL_ISR                ;define   NULL_ISR
        .def    WD_Disable              ;define   WD_Disable
        .def    _DSP28x_usDelay         ;define   _DSP28x_usDelay externally refered

        .ref    _c_int00                ;refer to function externally defined
        .global _DSP28x_usDelay         ;declare global function or variables
        .global _SetDBGIER

;-------------------------------------------------------------------------------
; CPU Interrupt Vector Table
;
; 32 interrupt vector addresses - Each 32 bits long.
; - First 32 bits = 24-bit address of Interrupt Service Routine (ISR).
; - Second 32 bits executed before transferring control to the ISR.
; - Must be aligned on a 256 boundary.
;-------------------------------------------------------------------------------
        .sect   ".intvectbl"
        .align  256

RESETIV:  .long RESET_ISR       ;Point Reset Vector to C Environment Entry Point
IV01:     .long NULL_ISR        ; Maskable hardware interrupt
IV02:     .long NULL_ISR        ; Maskable hardware interrupt
IV03:     .long NULL_ISR        ; Maskable hardware interrupt
IV04:     .long NULL_ISR        ; Maskable hardware interrupt
IV05:     .long NULL_ISR        ; Maskable hardware interrupt
IV06:     .long NULL_ISR        ; Maskable hardware interrupt
IV07:     .long NULL_ISR        ; Maskable hardware interrupt
IV08:     .long NULL_ISR        ; Maskable hardware interrupt
IV09:     .long NULL_ISR        ; Maskable hardware interrupt
IV10:     .long NULL_ISR        ; Maskable hardware interrupt
IV11:     .long NULL_ISR        ; Maskable hardware interrupt
IV12:     .long NULL_ISR        ; Maskable hardware interrupt
IV13:     .long NULL_ISR        ; Maskable hardware interrupt
IV14:     .long NULL_ISR        ; Maskable hardware interrupt
IV15:     .long NULL_ISR        ; DLOGINT
IV16:     .long NULL_ISR        ; RTOSINT
IV17:     .long NULL_ISR        ; Reserved
IV18:     .long NULL_ISR        ; NMI
IV19:     .long NULL_ISR        ; Illegal Instruction Trap
IV20:     .long NULL_ISR        ; User defined Software Interrupt
IV21:     .long NULL_ISR        ; User defined Software Interrupt
IV22:     .long NULL_ISR        ; User defined Software Interrupt
IV23:     .long NULL_ISR        ; User defined Software Interrupt
```

Figure 16.22 Example of start-up code.

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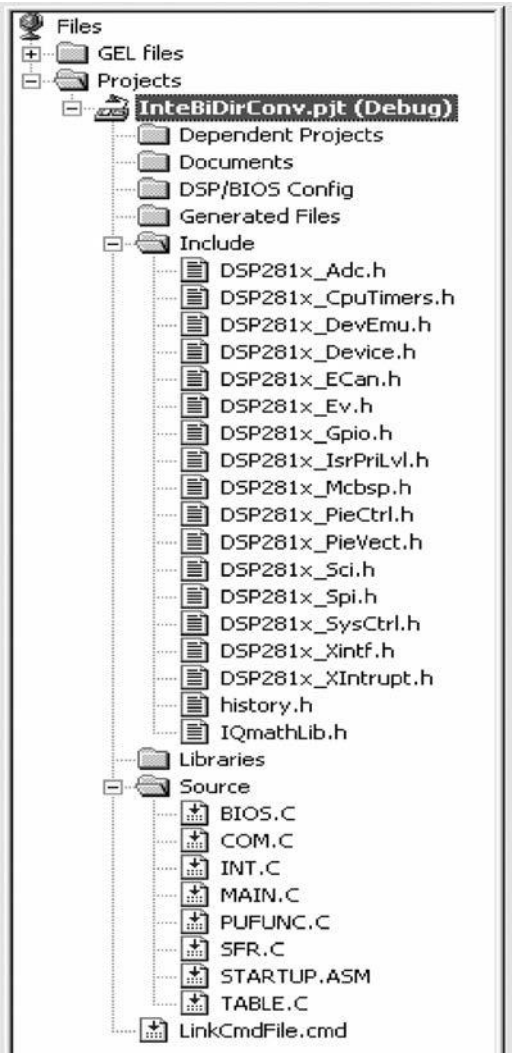


Figure 16.23 Header files and source modules.

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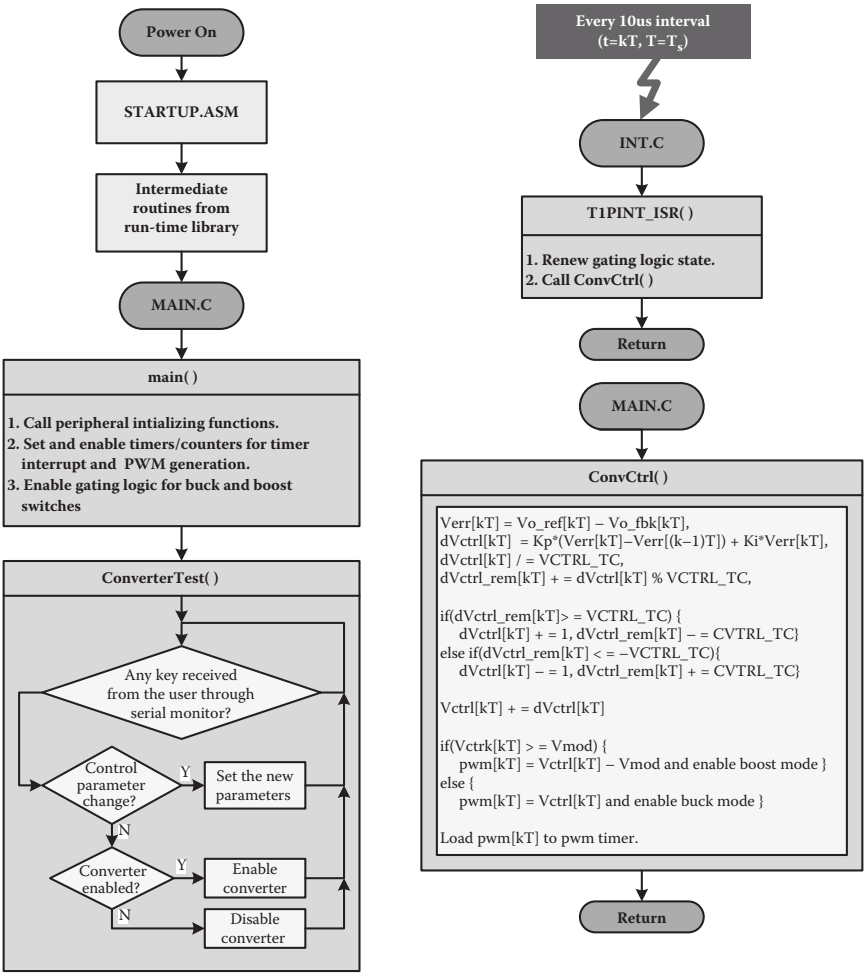


Figure 16.24 Control flow chart to construct control routines.

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A. MAIN.C

```
void main(void) {
//-------------------------------------------------------------------------------
//--- Initialize direction and data registers for GPIO ports                  ---
//--- Set all GPIOs to input port to prevent actuators from                   ---
//---  being activated                                                        ---
//-------------------------------------------------------------------------------
        eallow();                       //protected register access allowed
        GPADIR.all = 0x0000;
        GPBDIR.all = 0x0000;
        GPDDIR.all = 0x0000;
        GPEDIR.all = 0x0000;
        GPFDIR.all = 0x0000;
        GPGDIR.all = 0x0000;
        GPADAT.all = 0xFFFF;
        GPBDAT.all = 0xFFFF;
        GPDDAT.all = 0xFFFF;
        GPEDAT.all = 0xFFFF;
        GPFDAT.all = 0xFFFF;
        GPGDAT.all = 0xFFFF;
        edis();                         //protected register access disabled

        InitPeripherals();              //initializes the peripherals to a default state by calling each initializing function

        enEN_244();                     //SN74HC244 enabled

        setPWM1Freq(SW_FREQ);           //set PWM1 frequency to 100kHz
        setPWM1Duty(10);                //set PWM1 to 10 to make Start of Conversion of ADCSEQ1
        enPWM1();                       //enable PWM1 operation
        enPWM1Timer();                  //enable PWM1 timer
        enPWM1out();                    //enable PWM1 output

        GATEMD = NULL_MD;               //
        setGATEMD(GATEMD);              //disable gating logic: turn off all switches
        rstGateOut();                   //disable G1_O ~ G6_O and clear internal latch
        enGateOut();                    //enable G1_O ~ G6_O
        setC_REF(10000);                //set C_REF to 10.000[A]

        ConverterTest();                //converter test
}


void ConverterTest(void) {

int Vo_volt = 0, Vo_fbk = 0, Vo_max = 0;

        PrintMsg(msg_ConverterTest);
        while(1) {
                if(key_fg) {            //any key received from the user through serial monitor?
                        switch(_getch()) {
                                case '1' :  if(CONVERTER_EN) {
                                                _printf("Disable converter first!!!\n"); }
                                            else {      _printf("Mode 1 selected.\n");
                                                IBCCTRL_MD = IBCCTRL_MD1; }
                                            break;
                                case '2' :  if(CONVERTER_EN) {
                                                _printf("Disable converter first!!!\n"); }
                                            else {      _printf("Mode 2 selected.\n");
                                                IBCCTRL_MD = IBCCTRL_MD2; }
                                            break;
                                case '3' :  if(CONVERTER_EN) {
                                                _printf("Disable converter first!!!\n"); }
                                            else {      _printf("Mode 3 selected.\n");
                                                IBCCTRL_MD = IBCCTRL_MD3; }
                                            break;
                                case 'c' :  DISCON_CMP_EN ^= 1;
                                            if(DISCON_CMP_EN) _printf("Discontinuity compensation enabled...\n");
                                            else              _printf("Discontinuity compensation disabled...\n");
```

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```
                                        break;
                                case 'l' :  LNR_CMP_EN ^= 1;
                                        if(LNR_CMP_EN)      _printf("Linearized compensation enabled...\n");
                                        else                _printf("Linearized compensation disabled...\n");
                                        break;
                                case 's' :  if(!CONVERTER_EN) {
                                                _printf("Converter enabled...\n");
                                                CONVERTER_EN = 1; }
                                        else {      _printf("Converter disabled...\n");
                                                CONVERTER_EN = 0; }
                                break;
                                case '+' :  if(IBCCTRL_MD == IBCCTRL_MD1 || IBCCTRL_MD == IBCCTRL_MD3) {
                                                if(Vbatt_volt + 5 < VBATT_LMT) {
                                                        Vbatt_volt += 5;
                                                        SetADC_ref(Vbatt_volt, VBATT_MAX, &Vbatt_ref);
                                                }
                                        }
                                        else if(IBCCTRL_MD == IBCCTRL_MD2) {
                                                if(Vhv_volt + 5 < VHV_LMT) {
                                                        Vhv_volt += 5;
                                                        SetADC_ref(Vhv_volt, VHV_MAX, &Vhv_ref);
                                                }
                                        }
                                        break;
                                case '-' :  if(IBCCTRL_MD == IBCCTRL_MD1 || IBCCTRL_MD == IBCCTRL_MD3) {
                                                if(Vbatt_volt >= 5)     {
                                                        Vbatt_volt -= 5;
                                                        SetADC_ref(Vbatt_volt, VBATT_MAX, &Vbatt_ref);
                                                }
                                        }
                                        else if(IBCCTRL_MD == IBCCTRL_MD2) {
                                                if(Vhv_volt >= 5) {
                                                        Vhv_volt -= 5;
                                                        SetADC_ref(Vhv_volt, VHV_MAX, &Vhv_ref);
                                                }
                                        }
                                        break;
                                case 'e' :  enGateOut();                _printf("%s", msg_ConverterTest[11]);    break;
                                case 'r' :  rstGateOut();               _printf("%s", msg_ConverterTest[12]);    break;
                                case 'x' :  CONVERTER_EN = 0;           _printf("%s", msg_ConverterTest[13]);    return;
                                case 'd' :  break;
                                default  :  _printf("\nInvalid key pressed\n");
                                        PrintMsg(msg_ConverterTest);
                                        break;
                        }
                        if(IBCCTRL_MD == IBCCTRL_MD1 || IBCCTRL_MD == IBCCTRL_MD3) {
                                Vo_volt = Vbatt_volt;
                                Vo_fbk  = Vbatt_fbk;
                                Vo_max  = VBATT_MAX;
                        }
                        else if(IBCCTRL_MD == IBCCTRL_MD2) {
                                Vo_volt = Vhv_volt;
                                Vo_fbk  = Vhv_fbk;
                                Vo_max  = VHV_MAX;
                        }
                        _printf("%d: %d: %d: %d: %d\n", Vo_volt, GetVoltAmp(Vo_fbk, Vo_max), Ictrl, Iref, Vctrl);
                }
        }
}


//-------------------------------------------------------------------------
//---                                                                   ---
//--- To control non-inverting buck-boost converter (NIBBC)             ---
//---                                                                   ---
//-------------------------------------------------------------------------
#define     VCTRL_TC3                   2560
```

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```
inline void NIBBCCtrl(void) {

long dPID;
int Verr, quot, Vbnd, Vlth;

        Vbatt_fbk  = SampleADCRESULT2(Vbatt_fbk);       //sample ADCRESULT2 with averaging filter
        Vhv_fbk   = SampleADCRESULT3(Vhv_fbk);          //sample ADCRESULT3 with averaging filter

        //--- when converter is disabled ---
        if(!CONVERTER_EN) {
                Ictrl = 0;
                Iref  = 0;
                Vctrl = 0;
                Verr1 = Verr2 = 0;
                rem_sum1 = 0;
                GATEMD   = NULL_MD;
                setGATEMD(GATEMD);
                goto CtrlEnd;
        }

        //--- Voltage control to generate Ictrl ---
        Verr = Vhv_ref - Vhv_fbk;

        dPID  = (long)Verr * V_GAIN + (long)(Verr - Verr1) * 100;
//      dPID  = (long)Verr * V_GAIN;
        quot   = (int)(dPID / VCTRL_TC3);
        rem_sum1  += (int)(dPID % VCTRL_TC3);
        if    (rem_sum1   >  VCTRL_TC3)          [29]
        else if(rem_sum1 < -VCTRL_TC3)           { quot--; rem_sum1 += VCTRL_TC3; }
        Vctrl  += quot;

        if    (Vctrl > BUCK_PWM_MAX + BOOST_PWM_MAX)        Vctrl = BUCK_PWM_MAX + BOOST_PWM_MAX;
        else if(Vctrl < PWM_LTH)                            Vctrl = PWM_LTH;

        Verr2 = Verr1;
        Verr1 = Verr;

        //---when discontinuity compensation enabled ---
        Vbnd = PWM_FULL - 2;
        Vlth = PWM_LTH  + 2;

        //--- set PWM value and gating logic according to the operation mode ---
        if(Vctrl <= Vbnd) {
                T1CMPR  = Vctrl;                        //reload PWM output value and effective at next T1PR IRQ
                GATEMD  = BUCK_MD1;
        }
        //--- boost ---
        else {
                T1CMPR  = Vctrl - Vbnd + Vlth;          //reload PWM output value and effective at next T1PR IRQ
                GATEMD  = BOOST_MD1;
        }
        //--- End of control ---
CtrlEnd:;
}
```

B. BIOS.C

```
//---------------------------------------------------------------------------
// InitPeripherals() :
//---------------------------------------------------------------------------
// The following function initializes the peripherals to a default state.
// It calls each of the peripherals default initialization functions.
// This function should be executed at boot time or on a soft reset.
//---------------------------------------------------------------------------
void InitPeripherals(void) {

        disable();                              //disable all interrupts at the CPU level

        InitDevEmu();                           //On F2812/F2810 TMX samples prior to rev C this initialization was
```

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```
                                        // required.  For Rev C and after this is no longer required
    DisWatchDog();                      //Disable the watchdog
    InitPLL(0xA);                       //Initialize the PLLCR to 0xA : CLKIN(30MHz) x 10 / 2 = 150MHz
    InitPeriphCLK();                    //Initialize the high/low speed peripheral clocks
    InitInterrupt();                    //initializes the PIE control registers : all PIE and CPU IRQ disabled

    //---------- ---------- ---------- ---------- ---------- ----------
    //--- copy the "RamFuncs" section for InitFlash()          ---
    //---------- ---------- ---------- ---------- ---------- ----------
    MemCopy(&RamFuncsLoadStart, &RamFuncsLoadEnd, &RamFuncsRunStart);
    InitFlash();                        //initialize flash ROM control register

    #if DSP28_F2812
    InitXIntf();                        //Initialize External Interface To default State
    #endif
    //---------- ---------- ---------- ---------- ----------
    //--- initialize GPIO control system             ---
    //---------- ---------- ---------- ---------- ----------
    InitGPIO();                         //Initializes the GPIO to a known state.
    InitInputSignal();                  //initialize digital/analog input signals
    InitOutputSignal();                 //initialize digital/analog output signals

    //---------- ---------- ---------- ---------- ----------
    //--- set CPU Timer 0, 1, and 2                  ---
    //---------- ---------- ---------- ---------- ----------
    InitCPUTimer();                     //Initialize CPU Timers To default State
    //--- set CPU Timer 0 to general purpose timer and enable its PIE IRQ ---
    SetCPUTimer(0, 500);                //set CPU Timier 0 to 500[us] interval
    enTINT0_PHP();                      //enable CPU Timer 0 IRQ at the peripheral level
    setACK1();                          //set INT1 group IRQ acknowledge
    enINT1();                           //enable INT1 group IRQ at the CPU level

    //--- set CPU Timer 1 to general purpose timer ---
//  SetCPUTimer(1, 100);                //set CPU Timier 1 to 500[us] interval
//  enINT13();                          //enable INT13 group IRQ at the CPU level

    //--- set CPU Timer 2 to general purpose timer ---
//  SetCPUTimer(2, 20);                 //set CPU Timier 2 to 500[us] interval
//  enINT14();                          //enable INT14 group IRQ at the CPU level

    //---------- ---------- ---------- ---------- ---------- ----------
    //--- set SCI-A, SCI-B to general UART operation   ---
    //---------- ---------- ---------- ---------- ---------- ----------
    InitSCI();                          //Initialize SCI Peripherals To default State
    //--- SCI_A : com. with external controller ---
    SetSCIUART(SCI_A, BD_38400,  DATA_8BIT | IDLE_MD | LPBK_DIS | PRTY_DIS | ODD_PRTY | STOP_1BIT);
    enSCIA_RXD();                       //enable SCIA RX
    enSCIA_TXD();                       //enable SCIA TX
    rstSCIA_RTX();                      //reset and release SCIA RTX channels
    rstSCIA_TXFFPNT();                  //reset and release SCIA TX FIFO pointer
    rstSCIA_RXFFPNT();                  //reset and release SCIA RX FIFO pointer
    enSCIRXINTA_SRC();                  //enable SCIA RXINT at the interrupt source level
    enSCITXINTA_SRC();                  //enable SCIA TXINT at the interrupt source level
    disSCIRXFFINTA_SRC();               //disable SCIA RXFFINT at the interrupt source level
    disSCITXFFINTA_SRC();               //disable SCIA TXFFINT at the interrupt source level
    enSCIRXINTA_PHP();                  //enable SCIA RX IRQ at the peripheral level
    enSCITXINTA_PHP();                  //enable SCIA TX IRQ at the peripheral level

    //--- SCI_B : for serial monitor for debugging ---
    SetSCIUART(SCI_B, BD_115200, DATA_8BIT | IDLE_MD | LPBK_DIS | PRTY_DIS | ODD_PRTY | STOP_1BIT);
    enSCIB_RXD();                       //enable SCIB RX
    enSCIB_TXD();                       //enable SCIB TX
    rstSCIB_RTX();                      //reset and release SCIB RTX channels
    rstSCIB_TXFFPNT();                  //reset and release SCIB TX FIFO pointer
    rstSCIB_RXFFPNT();                  //reset and release SCIB RX FIFO pointer

    enSCIRXINTB_SRC();                  //enable SCIB RXINT at the interrupt source level
    enSCITXINTB_SRC();                  //enable SCIB TXINT at the interrupt source level
    disSCIRXFFINTB_SRC();               //disable SCIB RXFFINT at the interrupt source level
    disSCITXFFINTB_SRC();               //disable SCIB TXFFINT at the interrupt source level
```

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```
        enSCIRXINTB_PHP();              //enable SCIB RX IRQ at the peripheral level
        enSCITXINTB_PHP();              //enable SCIB TX IRQ at the peripheral level

        setACK9();                      //set INT9 group IRQ acknowledge at the peripheral level
        enINT9();                       //enable INT9 group IRQ at the CPU level

        //-----------------------------------------------------------
        //--- Initialize SPI Peripherals To default State ---
        //-----------------------------------------------------------
        InitSPI();

        //-------------------------------------------------------------
        //--- Initialize McBSP Peripheral To default State ---
        //-------------------------------------------------------------
        InitMcBSP();

        //-------------------------------------------------------
        //--- intialize ADC                 ---
        //-------------------------------------------------------
        InitADC();                      //Initialize ADC Peripheral To default State
        StartADCSEQ();                  //start ADC SEQ  sequencer in cascaded mode
//      enADCSEQINT_SRC();              //enable ADC SEQ1 IRQ at source level
//      enADCINT_PHP();                 //enable ADC IRQ at the peripheral level
//      setACK1();                      //set INT1 group IRQ acknowledge
//      enINT1();                       //enable INT1 group IRQ at the CPU level

        //-------------------------------------------------------
        //--- intialize eCAN                ---
        //-------------------------------------------------------
        InitCAN();                      //Initialize eCAN Peripheral To default State

        //-------------------------------------------------------
        //--- intialize event manager       ---
        //-------------------------------------------------------
        InitEV();                       //Initialize Event Manager Peripheral To default State

        disT1();                        //T1 operation enabled
        disT1CMP();                     //T1 compare operation enabled
        disT1CMPOE();                   //T1 compare output enabled

        disT2();                        //T2 operation disabled
        disT2CMP();                     //T2 compare operation disabled
        disT2CMPOE();                   //T2 compare output disabled

        enT1PINT_SRC();                 //enable T1 period IRQ at interrupt source level
        enT1PINT_PHP();                 //enable T1 period IRQ at the peripheral level

        enT2PINT_SRC();                 //disable T2 period IRQ at interrupt source level
        enT2PINT_PHP();                 //disable T2 period IRQ at the peripheral level

        setACK2();                      //set INT2 group IRQ acknowledge
        setACK3();                      //set INT3 group IRQ acknowledge
        enINT2();                       //enable INT2 group IRQ at the CPU level
        enINT3();                       //enable INT3 group IRQ at the CPU level

        enable();                       //enable all CPU IRQ at the CPU level
}
```

C. COM.C

```
//-----------------------------------------------------------------------
// InitSCI() : This function initializes the SCI(s) to a known state.
//-----------------------------------------------------------------------
void InitSCI(void) {

uint BRR;
```

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```
//--------- ---------- ---------- ---------- --------
//--- Initialize SCI-A:
//--------- ---------- ---------- ---------- --------
//--- SCICCR            : Communications control register ---
SCIACCR.bit.SCICHAR  = 7;              //0 : the length of data = SCICHAR + 1 [bit]
                                                                  //1 :
                                                                  //2 :
SCIACCR.bit.ADDRIDLE_MODE = 0;         //3 : 0(idle line mode for RS-232), 1(address-bit mode for multi processor)
SCIACCR.bit.LOOPBKENA  = 0;            //4 : loop-back test     disabled(0)/enabled(1)
SCIACCR.bit.PARITYENA  = 0;            //5 : parity             disabled(0)/enabled(1)
SCIACCR.bit.PARITY  = 0;               //6 : parity bit         odd (0)/even(1)
SCIACCR.bit.STOPBITS  = 0;             //7 : stop bit           1-bit(0)/2-bit  (1)

//--- SCICTL1 : Control register 1 ---
SCIACTL1.bit.RXENA  = 0;               //0 : RX     disabled(0)/enabled(1)
SCIACTL1.bit.TXENA  = 0;               //1 : TX     disabled(1)/enabled(1)
SCIACTL1.bit.SLEEP  = 0;               //2 : sleep mode                 disabled(0)/enabled(1)
SCIACTL1.bit.TXWAKE  = 0;              //3 : TX wakeup method           not used(0)/used  (1)
                                       //4 : reserved
SCIACTL1.bit.SWRESET        = 1;       //5 : software reset     reset(0)/released(1)
SCIACTL1.bit.RXERRINTENA  = 0;         //6 : RX error IRQ       disabled(0)/enabled(1)
                                       //7 : reserved

//--- SCI baud rate selection register ---
BRR = (uint)(LOSPDCLK / (38400 * 8) - 1);          //default baud rate 38400 bps
SCIAHBAUD = BRR & 0xFF00;                          //SCIHBAUD: Baud rate (high) register : upper 8bit used
SCIALBAUD = BRR & 0x00FF;                          //SCILBAUD: Baud rate (low ) register : lower 8bit used

//--- SCIACTL2 : control register 2 ---
SCIACTL2.bit.TXINTENA       = 0;       //0 : TX     IRQ         disabled (0)/enabled(1)
SCIACTL2.bit.RXBKINTENA   = 0;         //1 : RX/BRK IRQ         disabled (0)/enabled(1)
                                       //2 : reserved
                                       //3 : reserved
                                       //4 : reserved
                                       //5 : reserved
//      SCIACTL2.bit.TXEMPTY        = 1;       //6 : TX transmisstion buffer   not empty(0)/empty  (1)
//      SCIACTL2.bit.TXRDY          = 1;       //7 : mark that TX data buffer  not ready(0)/ready  (1)

//--- Recieve status register ---
                                       //0 : reserved
//      SCIARXST.bit.RXWAKE         = 0;       //1 : Receiver wakeup detect flag              no(0)/yes (1)
//      SCIARXST.bit.PE     = 0;               //2 : Parity   error  flag                     no error(0)/error(1)
//      SCIARXST.bit.OE     = 0;               //3 : Overrun  error  flag                     no error(0)/error(1)
//      SCIARXST.bit.FE     = 0;               //4 : Framing  error  flag                     no error(0)/error(1)
//      SCIARXST.bit.BRKDT  = 0;               //5 : Break    detect flag                     no break(0)/break(1)
//      SCIARXST.bit.RXRDY  = 0;               //6 : Data ready to be read from SCIRXBUF      no(0)/yes (1)
//      SCIARXST.bit.RXERROR = 0;              //7 : Receiver error  flag                     no error(0)/error(1)

//--- Recieve emulation buffer register : 8 bit ---
//      SCIARXEMU = 0x0000;

//--- Recieve data buffer ---
//      SCIARXBUF.bit.RXDT = 0x00;             //0 ~ 7 : Received data byte(8 bit)
                                               //8 ~ 13: reserved
//      SCIARXBUF.bit.SCIFFPE = 0;             //14   : SCI PE error in FIFO mode : error(1)/no error(0)
//      SCIARXBUF.bit.SCIFFFE = 0;             //15   : SCI FE error in FIFO mode : error(1)/no error(0)

//--- Transmit data buffer : 8 bit ---
//      SCIATXBUF = 0x00;

//--- FIFO transmit register ---
SCIAFFTX.bit.TXFFILIL = 0;             //0 ~ 4 : TX FIFO IRQ level
SCIAFFTX.bit.TXFFIENA = 0;             //5    : TX FIFO IRQ                 disabled(0)/enabled(1)
SCIAFFTX.bit.TXINTCLR = 0;             //6    : Clear TX FIFO INT flag      nothing(0) /clear  (1)
//      SCIAFFTX.bit.TXFFINT  = 0;             //7    : TX FIFO IRQ flag            no(0)     /yes    (1)
//      SCIAFFTX.bit.TXFFST   = 0;             //8 ~ 12: FIFO status:  00000 - Transmit FIFO is empty.
                                               //                      00001 - Transmit FIFO has 1 words
                                               //                      00010 - Transmit FIFO has 2 words
                                               //                      00011 - Transmit FIFO has 3 words
```

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```
                                        //                      0xxxx - Transmit FIFO has x words
                                        //                      10000 - Transmit FIFO has 16 words
    SCIAFFTX.bit.TXFIFOXRESET = 0;      //13   : reset TX FIFO pointer(0) / TX FIFO re-enabled(1)
    SCIAFFTX.bit.SCIFFENA     = 0;      //14   : SCI FIFO enhancement disabled(0)/enabled(1)
    SCIAFFTX.bit.SCIRST       = 0;      //15   : SCI reset rx/tx channels(0) / RTX via SCI FIFO resumed(1)

    //--- FIFO recieve register ---
    SCIAFFRX.bit.RXFFIL       = 0;      //0 ~ 4 : RX FIFO Interrupt level
    SCIAFFRX.bit.RXFFIENA     = 0;      //5    : RX FIFO Interrupt          disabled(0)/enabled(1)
    SCIAFFRX.bit.RXFFINTCLR   = 0;      //6    : Clear TX FIFO IRQ flag     nothing (0)/clear  (1)
//  SCIAFFRX.bit.RXFFINT      = 0;      //7    : RX FIFO IRQ flag           no IRQ  (0)/yes    (1)
//  SCIAFFRX.bit.RXFIFST      = 0;      //8 ~ 12: FIFO status:  00000 - Receive FIFO is empty
                                        //                      00001 - Receive FIFO has 1 word
                                        //                      00010 - Receive FIFO has 2 words
                                        //                      00011 - Receive FIFO has 3 words
                                        //                      0xxxx - Receive FIFO has x words
                                        //                      10000 - Receive FIFO has 16 words
    SCIAFFRX.bit.RXFIFORESET  = 0;      //13   : RX FIFO reset(0) / RX FIFO reenabled(1)
    SCIAFFRX.bit.RXFFOVRCLR   = 0;      //14   : Clear RX FIFO overflow             nothing(0)/clear(1)
//  SCIAFFRX.bit.RXFFOVF      = 0;      //15   : RX FIFO overflow                   no(0)/overflowed(1)

    //--- FIFO control register ---
    SCIAFFCT.bit.FFTXDLY = 10;          //0 ~ 7 : FIFO transmit delay (0 ~ 255 x SCI clock)
                                        //8 ~ 12: reserved
    SCIAFFCT.bit.CDC = 0;               //13   : Auto baud mode        disabled    (0)/enabled  (1)
    SCIAFFCT.bit.ABDCLR  = 0;           //14   : Auto baud clear       nothing     (0)/clear    (1)
//  SCIAFFCT.bit.ABD = 0;               //15   : Auto baud detect      not completed(0)/completed(1)

    //--- FIFO Priority control ---
                                        //0 ~ 2 : reserved
    SCIAPRI.bit.FREE = 0;               //3    : Free emulation suspend mode
    SCIAPRI.bit.SOFT = 1;               //4    : Soft emulation suspend mode
                                        //       (00 - Immediate stop on suspend)
                                        //       (10 - Complete current receive/transmit sequence before stopping)
                                        //       (X1 - Free run. Continues SCI operation regardless of suspend)
                                        //5 ~ 7 : reserved

    //-------------------------------------------------------
    //--- Initialize SCI-B:
    //-------------------------------------------------------
    //--- SCICCR            : Communications control register ---
    SCIBCCR.bit.SCICHAR  = 7;           //0 : the length of data = SCICHAR + 1 [bit]
                                        //1 :
                                        //2 :
    SCIBCCR.bit.ADDRIDLE_MODE = 0;      //3 : 0(idle line mode for RS-232), 1(address-bit mode for multi processor)
    SCIBCCR.bit.LOOPBKENA     = 0;      //4 : loop-back test disabled(0)/enabled(1)
    SCIBCCR.bit.PARITYENA     = 0;      //5 : parity        disabled(0)/enabled(1)
    SCIBCCR.bit.PARITY        = 0;      //6 : parity bit    odd    (0)/even   (1)
    SCIBCCR.bit.STOPBITS      = 0;      //7 : stop bit :    1-bit  (0)/2-bit  (1)

    //--- SCICTL1 : Control register 1 ---
    SCIBCTL1.bit.RXENA        = 0;      //0 : RX              disabled(0)/enabled(1)
    SCIBCTL1.bit.TXENA        = 0;      //1 : TX              disabled(1)/enabled(1)
    SCIBCTL1.bit.SLEEP        = 0;      //2 : sleep mode      disabled(0)/enabled(1)
    SCIBCTL1.bit.TXWAKE       = 0;      //3 : TX wakeup method  not used(0)/used  (1)
                                        //4 : reserved
    SCIBCTL1.bit.SWRESET      = 1;      //5 : software reset    reset  (0)/released(1)
    SCIBCTL1.bit.RXERRINTENA  = 0;      //6 : RX error IRQ      disabled(0)/enabled(1)
                                                                //7 : reserved

    //--- SCI baud rate selection register ---
    BRR = LOSPDCLK / (38400 * 8) - 1;   //default baud rate 115200 bps
    SCIBHBAUD = BRR & 0xFF00;           //SCIHBAUD: Baud rate (high) register : upper 8bit used
    SCIBLBAUD = BRR & 0x00FF;           //SCILBAUD: Baud rate (low ) register : lower 8bit used

    //--- SCIACTL2 : control register 2 ---
    SCIBCTL2.bit.TXINTENA     = 0;      //0 : TX    IRQ       disabled (0)/enabled(1)
    SCIBCTL2.bit.RXBKINTENA   = 0;      //1 : RX/BRK IRQ      disabled (0)/enabled(1)
                                        //2 : reserved
                                        //3 : reserved
```

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```
                                        //4 : reserved
                                        //5 : reserved
//      SCIBCTL2.bit.TXEMPTY  = 1;      //6 : TX transmisstion buffer   not empty(0)/empty  (1)
//      SCIBCTL2.bit.TXRDY = 1;         //7 : mark that TX data buffer  not ready(0)/ready  (1)

        //--- Recieve status register ---
                                        //0 : reserved
//      SCIBRXST.bit.RXWAKE = 0;        //1 : Receiver wakeup detect flag              no(0)/yes(1)
//      SCIBRXST.bit.PE     = 0;        //2 : Parity   error  flag                     no error(0)/error(1)
//      SCIBRXST.bit.OE     = 0;        //3 : Overrun  error  flag                     no error(0)/error(1)
//      SCIBRXST.bit.FE     = 0;        //4 : Framing  error  flag                     no error(0)/error(1)
//      SCIBRXST.bit.BRKDT  = 0;        //5 : Break    detect flag                     no break(0)/break(1)
//      SCIBRXST.bit.RXRDY  = 0;        //6 : Data ready to be read from SCIRXBUF no(0)/yes(1)
//      SCIBRXST.bit.RXERROR = 0;       //7 : Receiver error  flag                     no error(0)/error(1)

        //--- Recieve emulation buffer register : 8 bit ---
//      SCIBRXEMU = 0x0000;

        //--- Recieve data buffer ---
//      SCIBRXBUF.bit.RXDT = 0x00;      //0 ~ 7 : Received data byte(8 bit)
                                                        //8 ~ 13: reserved
//      SCIBRXBUF.bit.SCIFFPE = 0;      //14   : SCI PE error in FIFO mode : error(1)/no error(0)
//      SCIBRXBUF.bit.SCIFFFE = 0;      //15   : SCI FE error in FIFO mode : error(1)/no error(0)

        //--- Transmit data buffer : 8 bit ---
//      SCIBTXBUF = 0x00;

        //--- FIFO transmit register ---
        SCIBFFTX.bit.TXFFILIL = 0;      //0 ~ 4 : TX FIFO IRQ level
        SCIBFFTX.bit.TXFFIENA = 0;      //5    : TX FIFO IRQ              disabled(0)/enabled(1)
        SCIBFFTX.bit.TXINTCLR = 0;      //6    : Clear TX FIFO INT flag   nothing(0) /clear  (1)
//      SCIBFFTX.bit.TXFFINT  = 0;      //7    : TX FIFO IRQ flag         no(0)/yes(1)
//      SCIBFFTX.bit.TXFFST   = 0;      //8 ~ 12: FIFO status: 00000 - Transmit FIFO is empty.
                                        //                  00001 - Transmit FIFO has 1 words
                                        //                  00010 - Transmit FIFO has 2 words
                                        //                  00011 - Transmit FIFO has 3 words
                                        //                  0xxxx - Transmit FIFO has x words
                                        //                  10000 - Transmit FIFO has 16 words
        SCIBFFTX.bit.TXFIFOXRESET = 1;  //13   : reset TX FIFO pointer(0) / TX FIFO re-enabled(1)
        SCIBFFTX.bit.SCIFFENA     = 0;  //14   : SCI FIFO enhancement disabled(0)/enabled(1)
        SCIBFFTX.bit.SCIRST       = 0;  //15   : SCI reset rx/tx channels(0) / RTX via SCI FIFO resumed(1)

        //--- FIFO recieve register ---
        SCIBFFRX.bit.RXFFIL   = 0;      //0 ~ 4 : RX FIFO Interrupt level
        SCIBFFRX.bit.RXFFIENA  = 0;     //5    : RX FIFO Interrupt              disabled(0)/enabled(1)
        SCIBFFRX.bit.RXFFINTCLR = 0;    //6    : Clear TX FIFO IRQ flag         nothing (0)/clear  (1)
//      SCIBFFRX.bit.RXFFINT   = 0;     //7    : RX FIFO IRQ flag               no IRQ  (0)/yes    (1)
//      SCIBFFRX.bit.RXFIFST   = 0;     //8 ~ 12: FIFO status: 00000 - Receive FIFO is empty
                                        //                  00001 - Receive FIFO has 1 word
                                        //                  00010 - Receive FIFO has 2 words
                                        //                  00011 - Receive FIFO has 3 words
                                        //                  0xxxx - Receive FIFO has x words
                                        //                  10000 - Receive FIFO has 16 words
        SCIBFFRX.bit.RXFIFORESET = 0;   //13   : RX FIFO reset(0) / RX FIFO reenabled(1)
        SCIBFFRX.bit.RXFFOVRCLR  = 1;   //14   : Clear RX FIFO overflow         nothing(0)/clear(1)
//      SCIBFFRX.bit.RXFFOVF     = 0;   //15   : RX FIFO overflow               nothing(0)/overflowed(1)

        //--- FIFO control register ---
        SCIBFFCT.bit.FFTXDLY = 10;      //0 ~ 7 : FIFO transmit delay (0 ~ 255 x SCI clock)
                                        //8 ~ 12: reserved
        SCIBFFCT.bit.CDC     = 0;       //13   : Auto baud mode          disabled(0)/enabled  (1)
        SCIBFFCT.bit.ABDCLR  = 0;       //14   : Auto baud clear         nothing(0)/clear(1)
//      SCIBFFCT.bit.ABD     = 0;       //15   : Auto baud detect        not completed(0)/completed(1)

        //--- FIFO Priority control ---
                                        //0 ~ 2 : reserved
        SCIBPRI.bit.FREE = 0;           //3    : Free emulation suspend mode
        SCIBPRI.bit.SOFT = 1;           //4    : Soft emulation suspend mode
                                        //       (00 - Immediate stop on suspend)
                                        //       (10 - Complete current receive/transmit sequence before stopping)
```

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```
                                        //      (X1 - Free run. Continues SCI operation regardless of suspend)
                                        //5 ~ 7 : reserved
}


//-----------------------------------------
//--- set SCI to UART operation ---
//-----------------------------------------
void SetSCIUART(uchar SCI_NO, ulong BAUD_RATE, uchar MODE) {

uint BRR;

        BRR  = (uint)(LOSPDCLK / (BAUD_RATE * 8) - 1); //default baud rate 115200 bps

        if(SCI_NO == SCI_A) {
                SCIACCR.all = MODE;             //data length | address mode | loop-back | parity | parity bits | stop bits
                SCIAHBAUD = BRR & 0xFF00;       //SCIHBAUD: Baud rate (high) register : upper 8bit used
                SCIALBAUD = BRR & 0x00FF;       //SCILBAUD: Baud rate (low ) register : lower 8bit used
        }
        else if(SCI_NO == SCI_B) {
                SCIBCCR.all = MODE;             //data length | address mode | loop-back | parity | parity bits | stop bits
                SCIBHBAUD = BRR & 0xFF00;       //SCIHBAUD: Baud rate (high) register : upper 8bit used
                SCIBLBAUD = BRR & 0x00FF;       //SCILBAUD: Baud rate (low ) register : lower 8bit used
        }
}
```

D. INT.C

```
//--- EV-A ---
interrupt void T1PINT_ISR(void) {

        setGATEMD(GATEMD);              //set converter operating mode

        PWM2 = 1;                       //set PWM1 synchronization clock

        ConvCtrl();                     //IBC voltage/current control routine

        PWM2 = 0;

        rstT1PINT_PHP();                //reset T1PINT IRQ at peripheral level
        setACK2();                      //set INT2 group IRQ acknowledge
}
```

E. PUFUNC.C

```
//-----------------------------------------------------
//--- send a character through SCI-B UART ---
//-----------------------------------------------------
char _putch(char ch) {

        GTIMER1 = 10;
        GTIMER1_FG = 0;
        while(!SCIBCTL2.bit.TXRDY) {    //check if TX data buffer ready for 10ms
                if(GTIMER1_FG)
                        return 0x00;    //return 0x00 to mark data not transmitted
        }
        SCIBTXBUF = ch;
        return ch;                      //return transmitted data to mark transmisstion succeeded
}


//-----------------------------------------------------
//--- get a character through SC-B UART ---
```

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```
//--------- ---------- ---------- ---------- ---------- -
char _getch(void) {

        if(key_fg)                              //check if data ready to be read from SCIRX BUF
                key_val = key_code;             //return received data
        else     key_val = 0x00;                //return 0x00
        key_fg = 0;
        return key_val;
}


//--------- ---------- ---------- ---------- --
//--- printf() via SCI-B              ---
//--------- ---------- ---------- ---------- --
void _printf(char *form, ...) {

char buf[128];                                  //total 128 character display
int i, j;
va_list  argptr;

        va_start(argptr, form);
        vsprintf(buf, form, argptr);            //copy string to buf[] according to form
        j = strlen(buf);
        for(i = 0; i < j; i++)  _putch(buf[i]);
        va_end(argptr);
}


//--------- ---------- ---------- ---------- --
//--- wait serial key stroke          ---
//--------- ---------- ---------- ---------- --
void _waitkey(char key) {

char ch;

        while(1) {
                if(key_fg) {
                        ch = _getch();
                        if(key >= 'A' && key <= 'Z')    key += 'a' - 'A';
                        if(ch  >= 'A' && ch  <= 'Z')    ch  += 'a' - 'A';
                        if(ch == key) break;
                }
        }
}
```

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16.3.7 Making and Running Executable Code File

An example of making a code file executable on TMS320F2812 is shown in this section. The software development environment is based on Code Composer Studio version 3.10 (CCS v3.10), which is provided by Texas Instruments. In order to download the user program, F28xx On-Chip Flash Programmer plug-in module for CCS v3.10 is used. The steps for downloading and running the user program on the TMS320F2812 DSP chip are shown in Figure 16.25a to i. For the detail usages, Reference 29 is helpful.

16.3.8 Testing Operation of Non-inverting Buck-Boost Converter

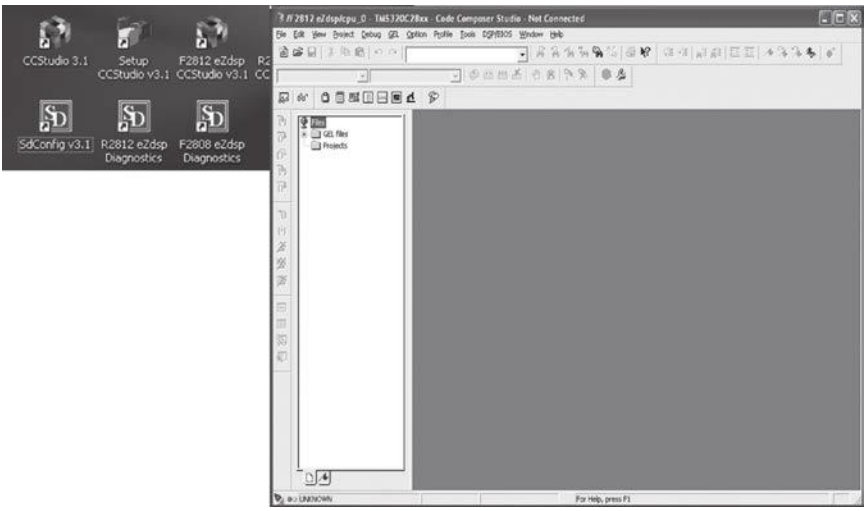
The electrical specifications to test the built non-inverting buck-boost converter and the digital controller with TM320F2812 DSP chip are given in Table 16.2. Figure 16.26a shows the expected output voltage waveform with regard to the input voltage variation. The waveforms in Figures 16.26b through d are the close-ups of the critical region. These waveforms help verify the stability and continuity of the DC gain of the large signal model in Figure 16.6.

Figure 16.27 presents screenshots of a serial monitor to help the programmer watch the operations of the program on the DSP chip. By using the serial monitor through the RS-232 with a personal computer, the programmer is able to implement a console.

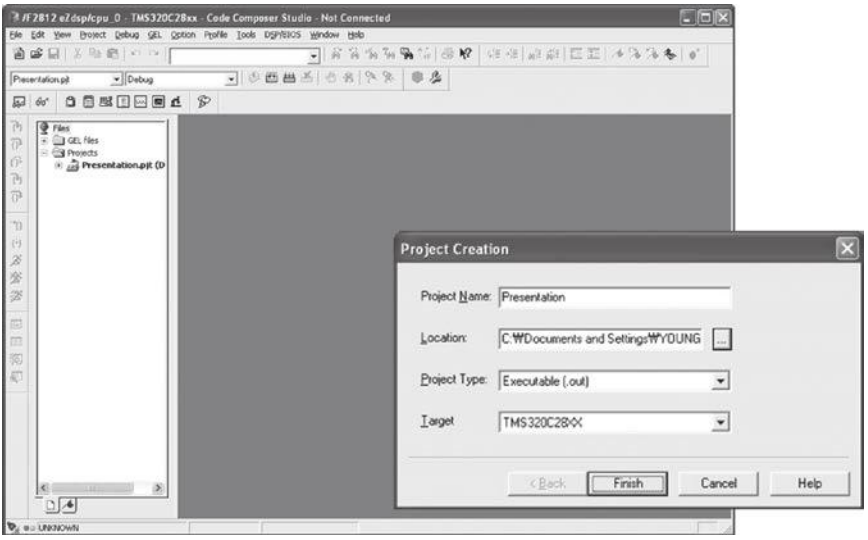
16.4 Summary

In this chapter, a series of preparatory steps and procedures for the implementation of a digital controller based on DSPs was overviewed. To better explain, the implementation of a non-inverting buck-boost converter was presented as an example with experimental results and suggestions to monitor the operation of a user program. Several schematics and source codes were provided as well.

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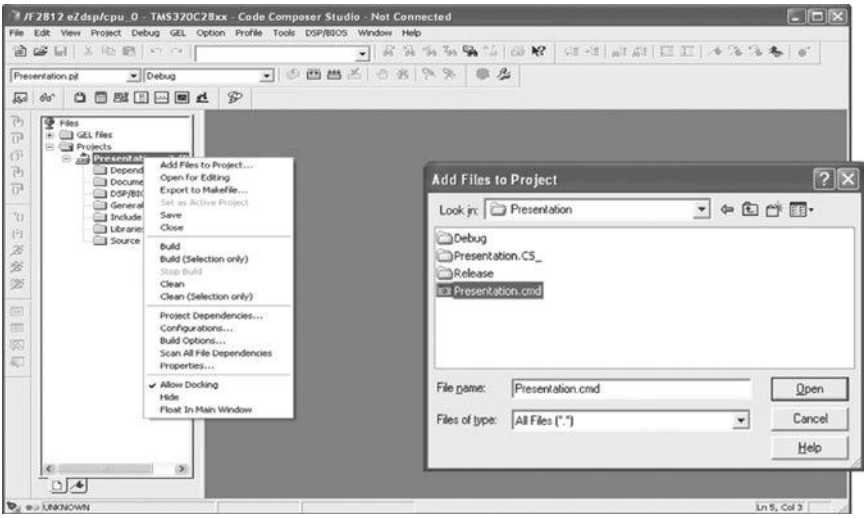
(a) Run CCS v3.10



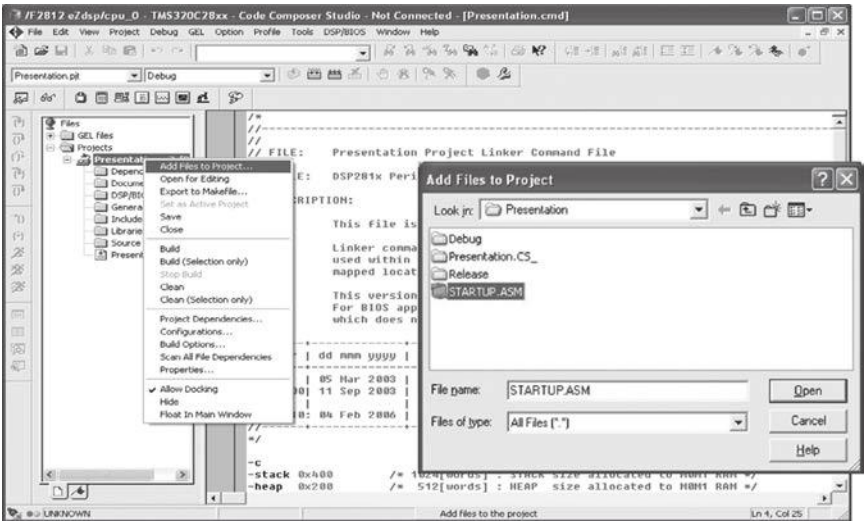
(b) Select Project –> New

Figure 16.25 An example of making and running a user program code on TMS320F2812 DSP chip. (a) Run CCS v3.10. (b) Select project -> New. (c) Add link command file to project tree. (d) Add start-up code to project tree. (e) Add user C/C++ source files to project tree. (f) Add run-time library to project tree. (g) Click "Rebuild All" button to generate an executable code file. (h) Click "F28xx On-Chip Flash Programmer" to download the generated code file. (i) Run the downloaded user program code.

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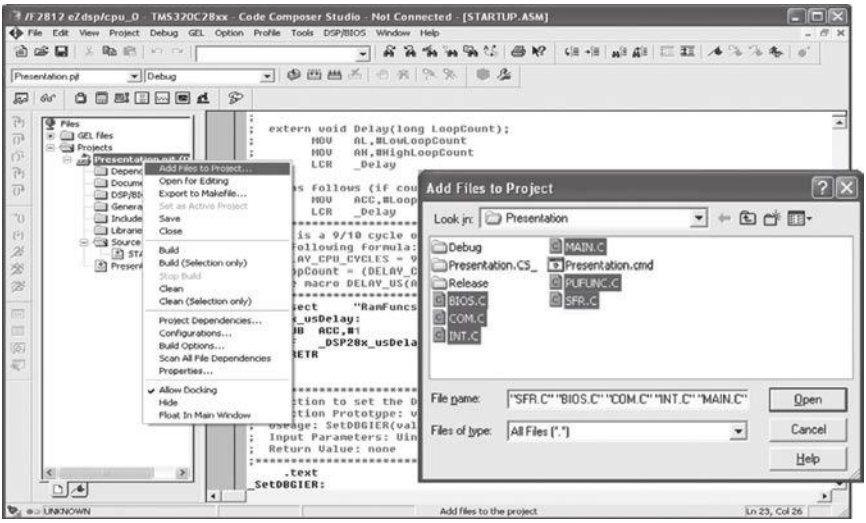
(c) Add Link Command File to Project Tree



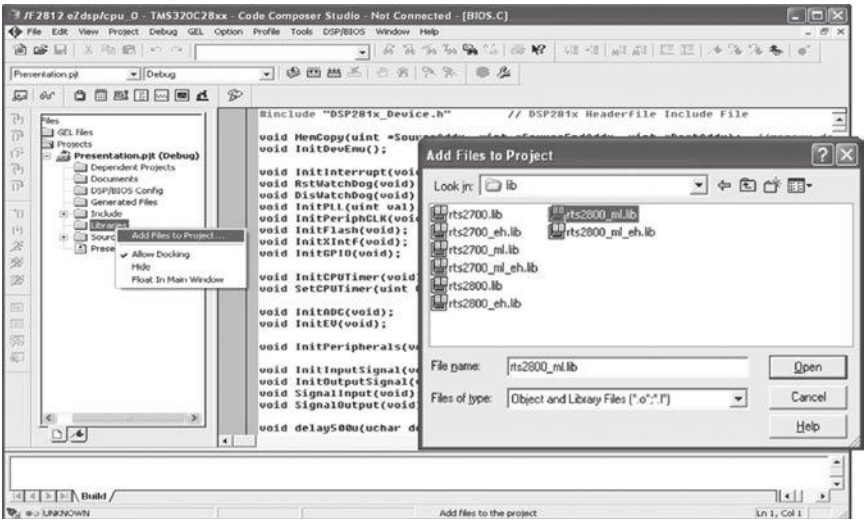
(d) Add Start-up Code to Project Tree

Figure 16.25 (continued)

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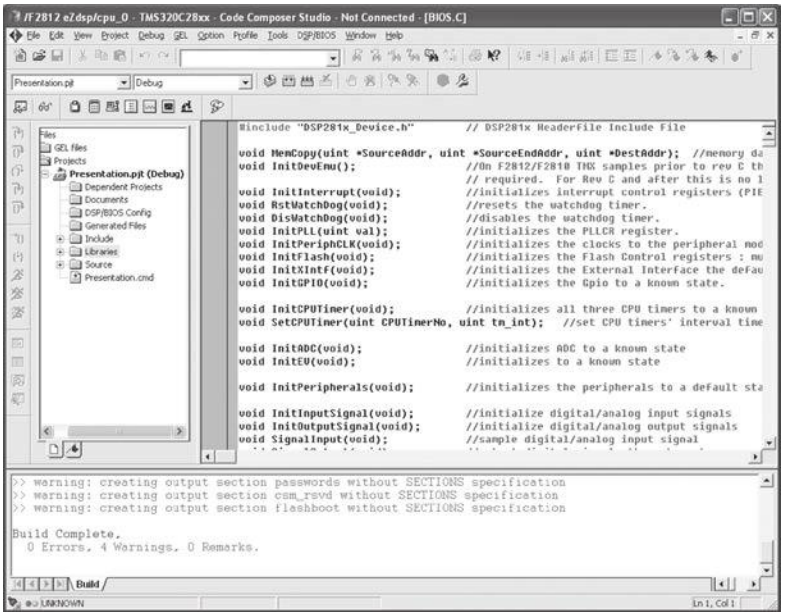
(e) Add User C/C++ Source Files to Project Tree



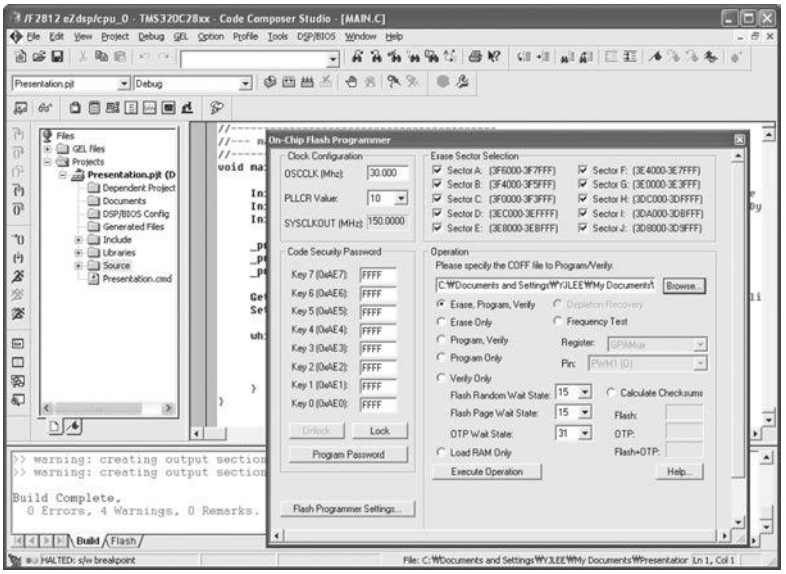
(f) Add Run-time Library to Project Tree

Figure 16.25 (continued)

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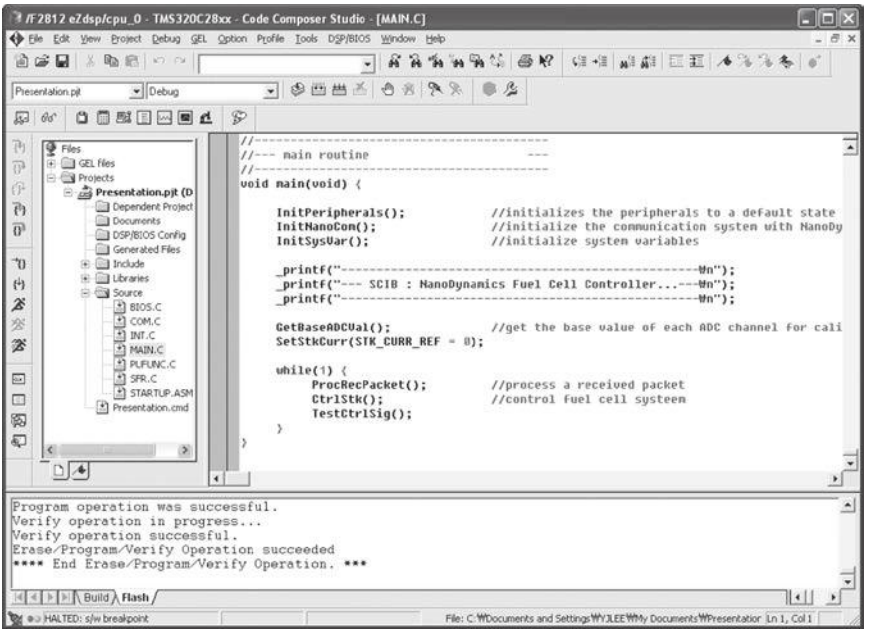
(g) Click Rebuild All Button to Generate an Executable Code File



(h) Click F28xx On-Chip Flash Programmer to Download the Generated Code File

Figure 16.25 (continued)

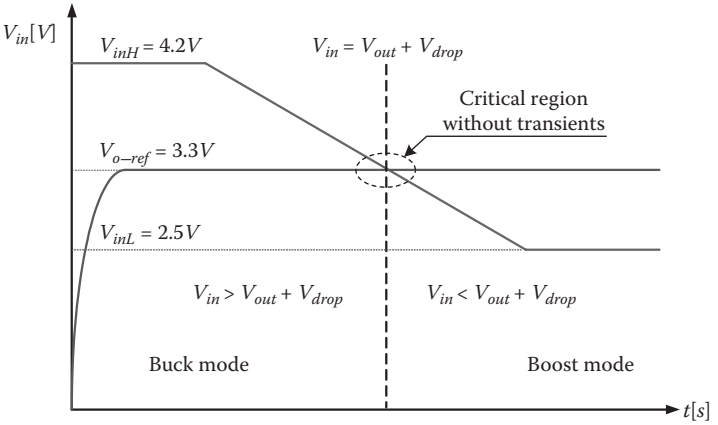
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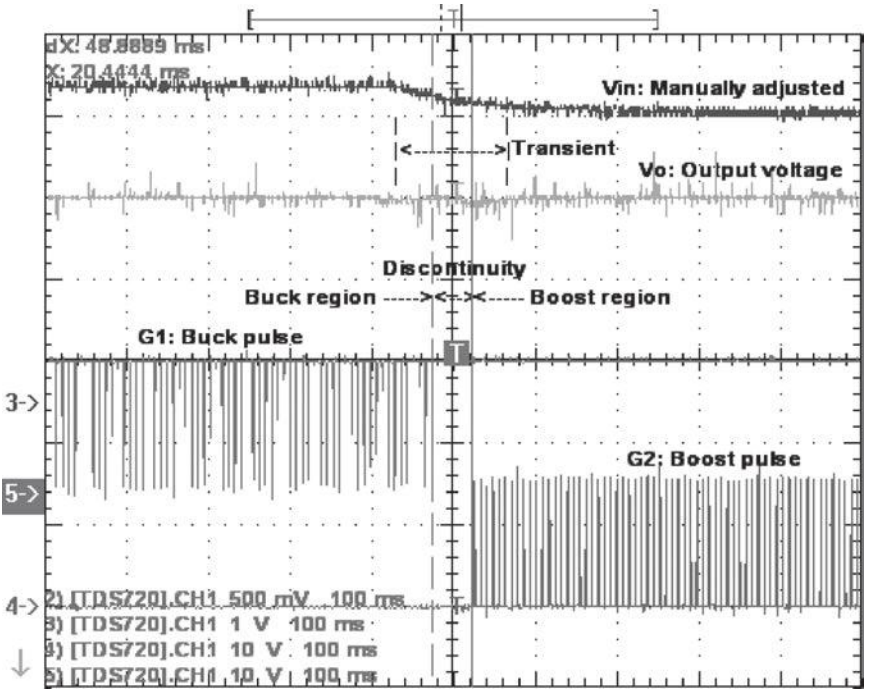
(i) Run the Downloaded User Program Code

Figure 16.25 (continued)

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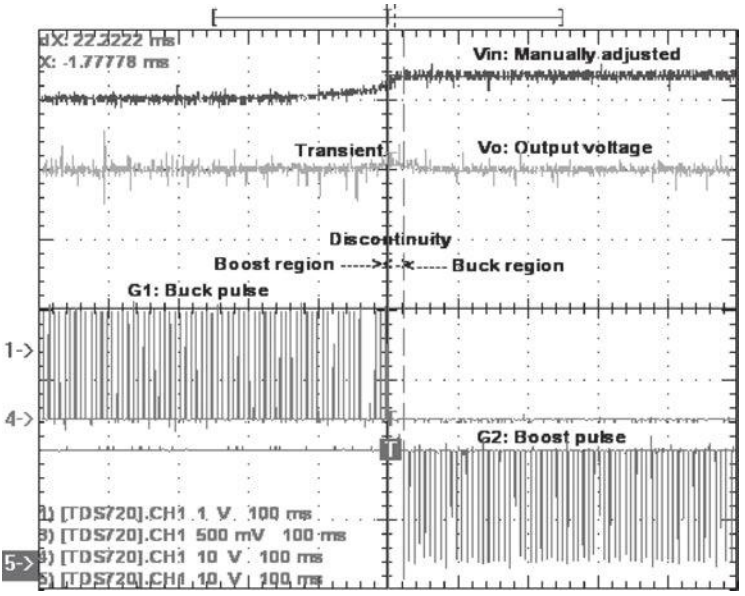
(a) An Expected Output Voltage Depending on the Input Voltage Variation



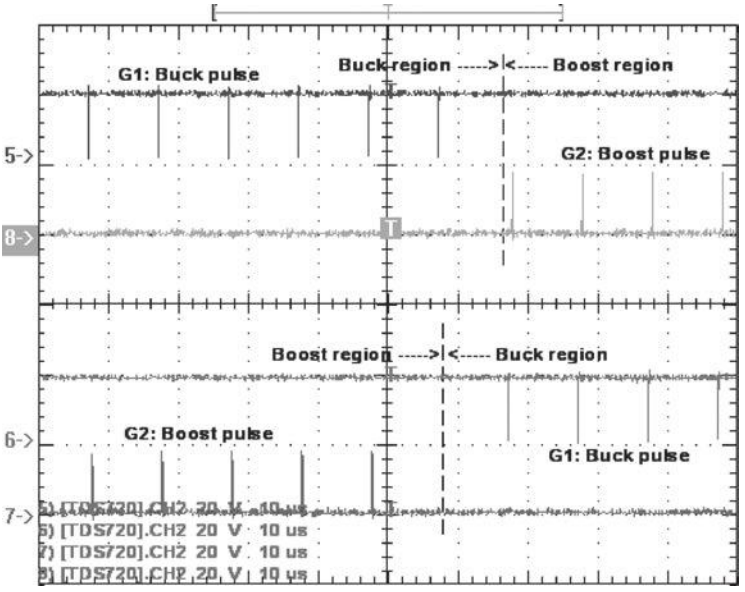
(b) Output Voltage During Smooth Transition from Buck to Boost

Figure 16.26 The expected and actual output voltages in the critical region. (a) An expected output voltage depending on the input voltage variation. (b) Output voltage during smooth transition from buck to boost. (c) Output voltage during smooth transition from boost to buck. (d) A close-up of the gating signal during smooth transition.

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(c) Output Voltage During Smooth Transition from Boost to Buck



(d) A Close-up of the Gating Signal During Smooth Transition

Figure 16.26 (continued)

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```
CONNECTED TO SERIAL PORT COM2 (115200-8N1)

 PWM_MAX=750, PWM_FULL=707, BUCK_PWM_MAX=706, BOOST_PWM_MAX=353
Read System Parameters...
0000 : 0050 02FC 0DB9

//-------------------------------------------------------------//
//--- Integrated Bi-directional AC/DC and DC/DC Converter ---//
//--- '1' : Buck and boost for Plug-in charging of battery---//
//--- '2' : Boost for discharging of battery               ---//
//--- '3' : Buck for regenerative charging of battery      ---//
//--- 'c' : Enable/disable discontinuity compensation      ---//
//--- 'l' : Enable/disable linearization                   ---//
//--- 's' : Enable/disable converter                       ---//
//--- '+' : Increase Voref                                 ---//
//--- '-' : Decrease Voref                                 ---//
//--- 'e' : Enable G1_O ~ G6_O output                      ---//
//--- 'r' : Disable G1_O ~ G6_O and clear internal latch   ---//
//--- 'x' : Exit                                           ---//
//-------------------------------------------------------------//
Mode 1 selected.
0: 0: 0: 0: 0
Discontinuity compensation enabled...
0: 0: 0: 0: 0
Converter enabled...
0: 0: 0: 0: 0
Converter disabled...
0: 0: 0: 0: 47
5: 0: 0: 0: 0
10: 0: 0: 0: 0
15: 0: 0: 0: 0
20: 0: 0: 0: 0
25: 0: 0: 0: 0
```

Figure 16.27 Example of serial monitoring for user program for TMS320F2812 chip.

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